SPECCTRAQuest Foundations

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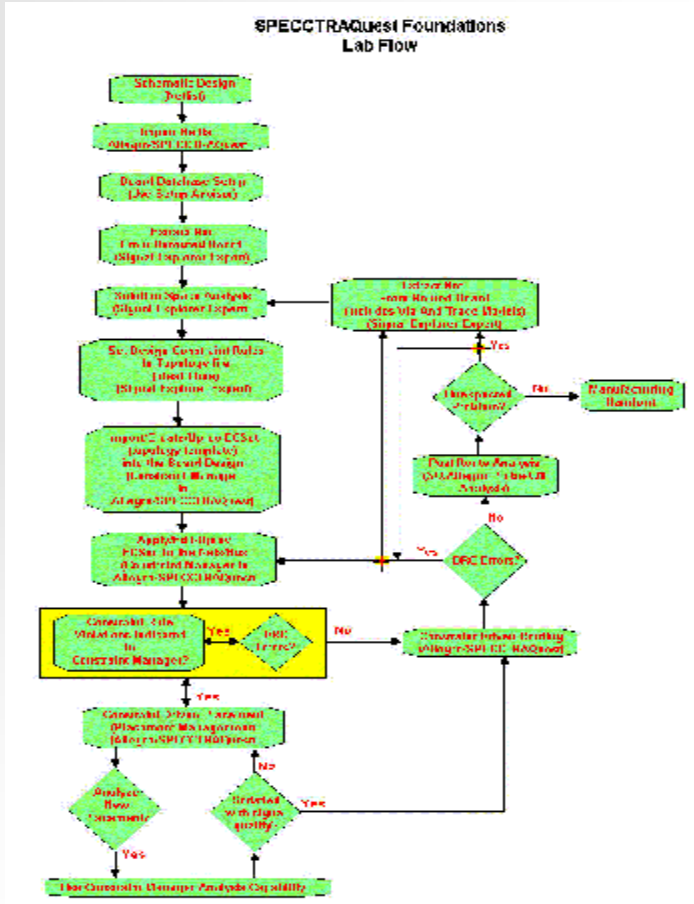
The SPECCTRAQuest Design Flow

The SPECCTRAQuest Design Flow consists of the following six steps:

Pre-Placement
Solution Space Analysis
Constraint-Driven Floorplanning
Constraint-Driven Routing
Post-Route DRC
Post-Route Analysis



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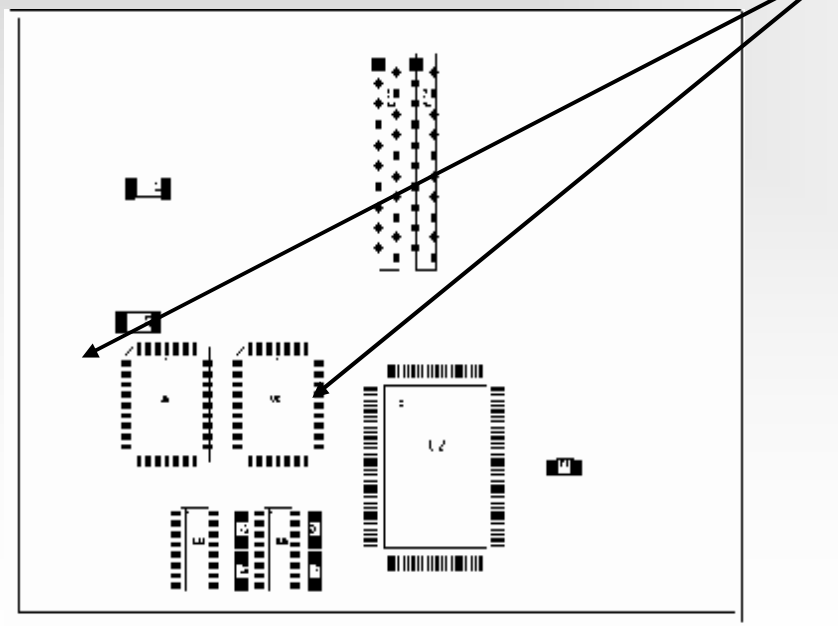
Design Flow: Pre-Placement

Standard form factors, mechanical restrictions, and standard practices often predefine locations of critical components.

Electrical design must start with these requirements, or present a strong case why things should be changed.

Pre-placed design is usually created by the CAD group as a starting point for design.



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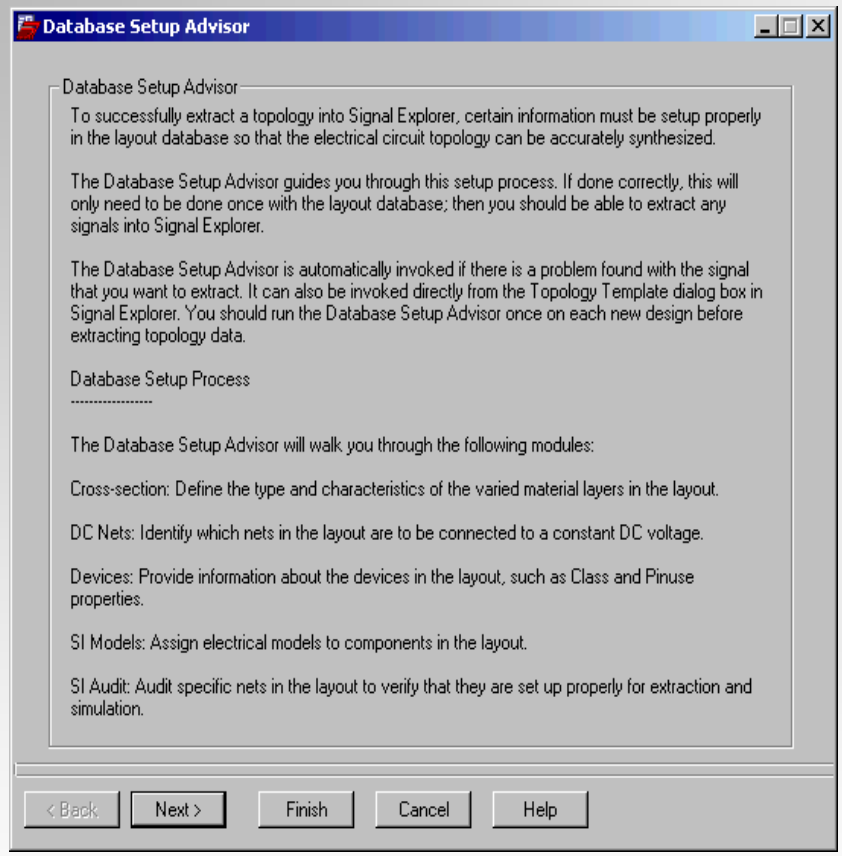
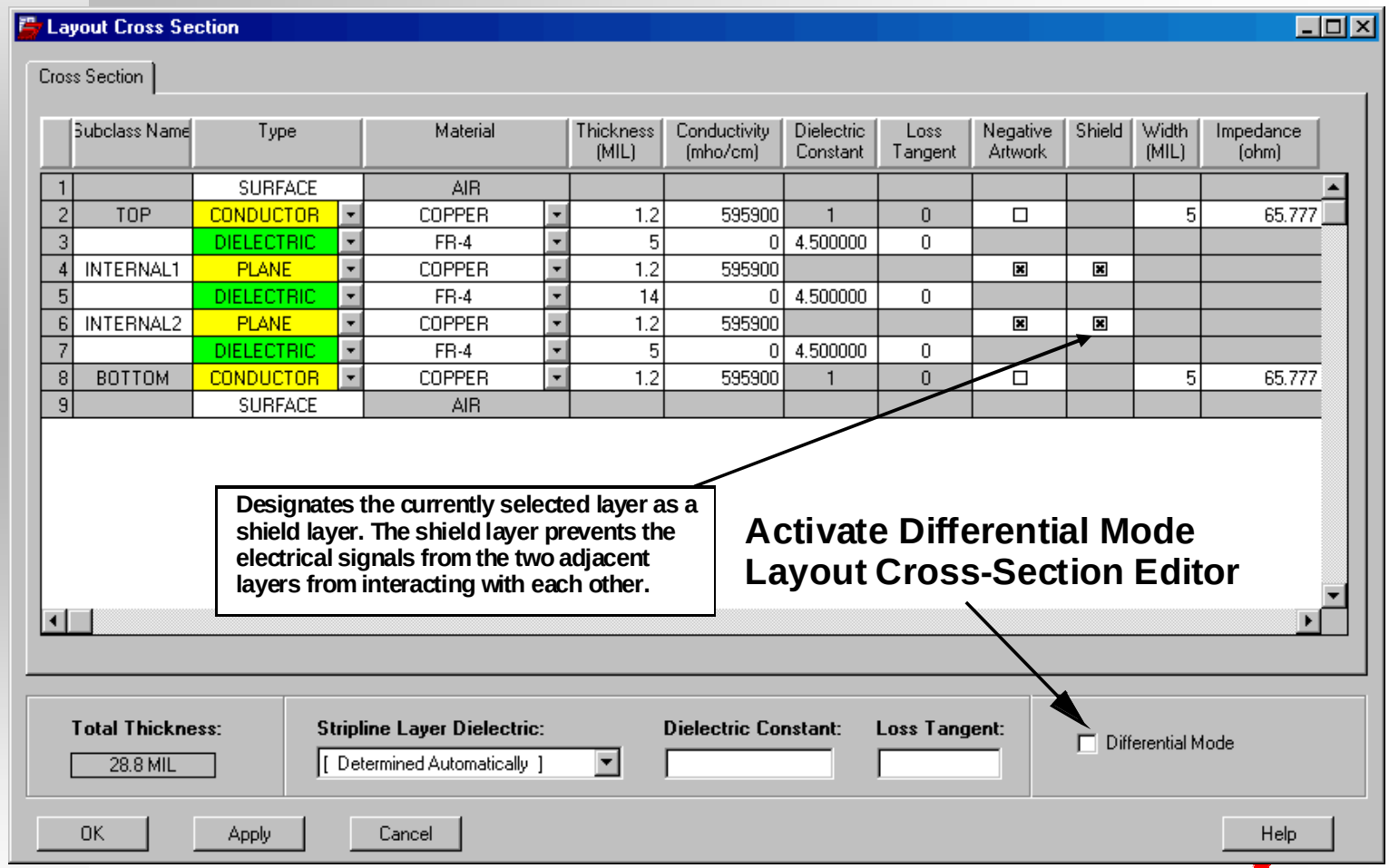
Database Setup Advisor



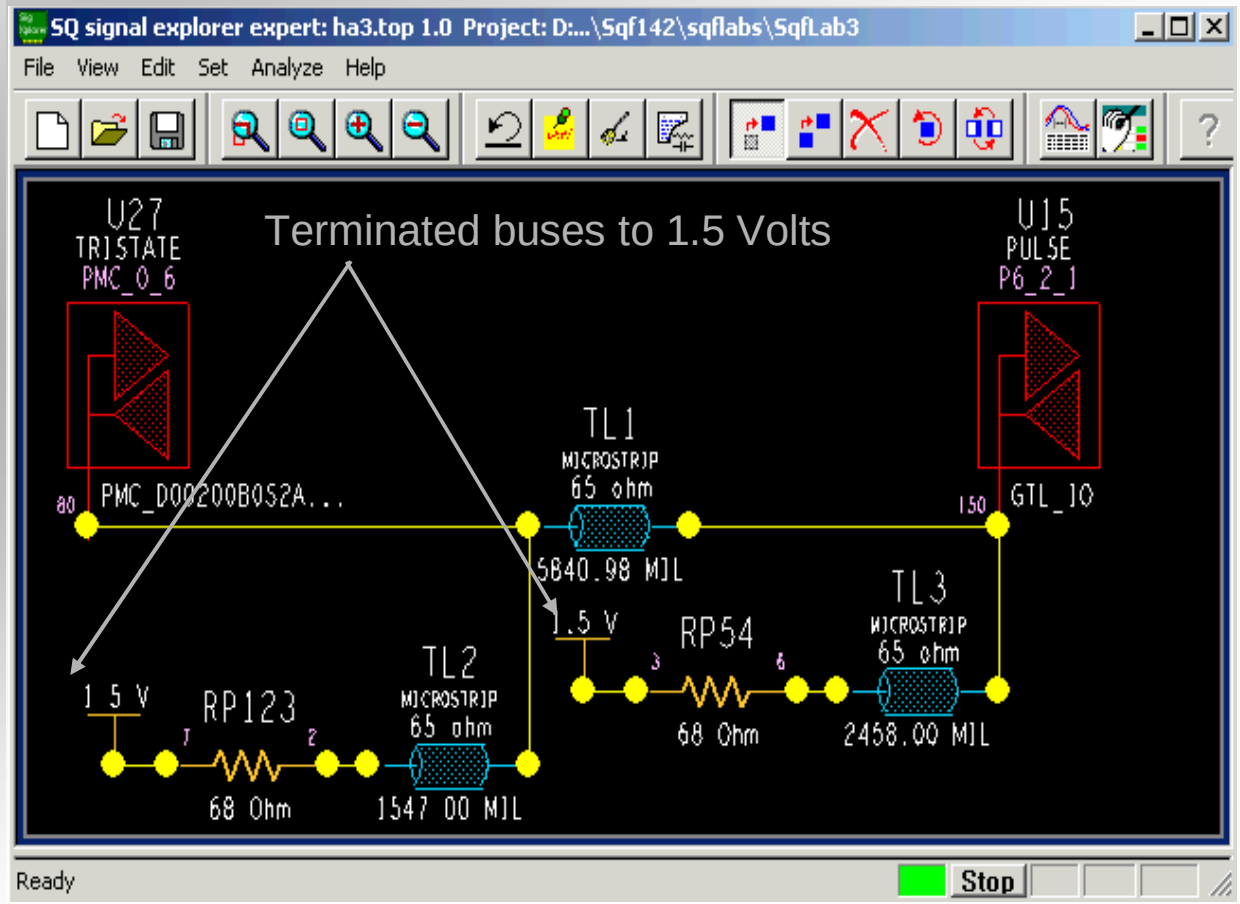
- The first screen of the Database Seup Advisor.
- Explains the use of Database Setup Advisor.
- Describes the steps you must take to set up the database correctly.
- “Set up Right, Set up Once”.

Defining the Layout Cross-Section

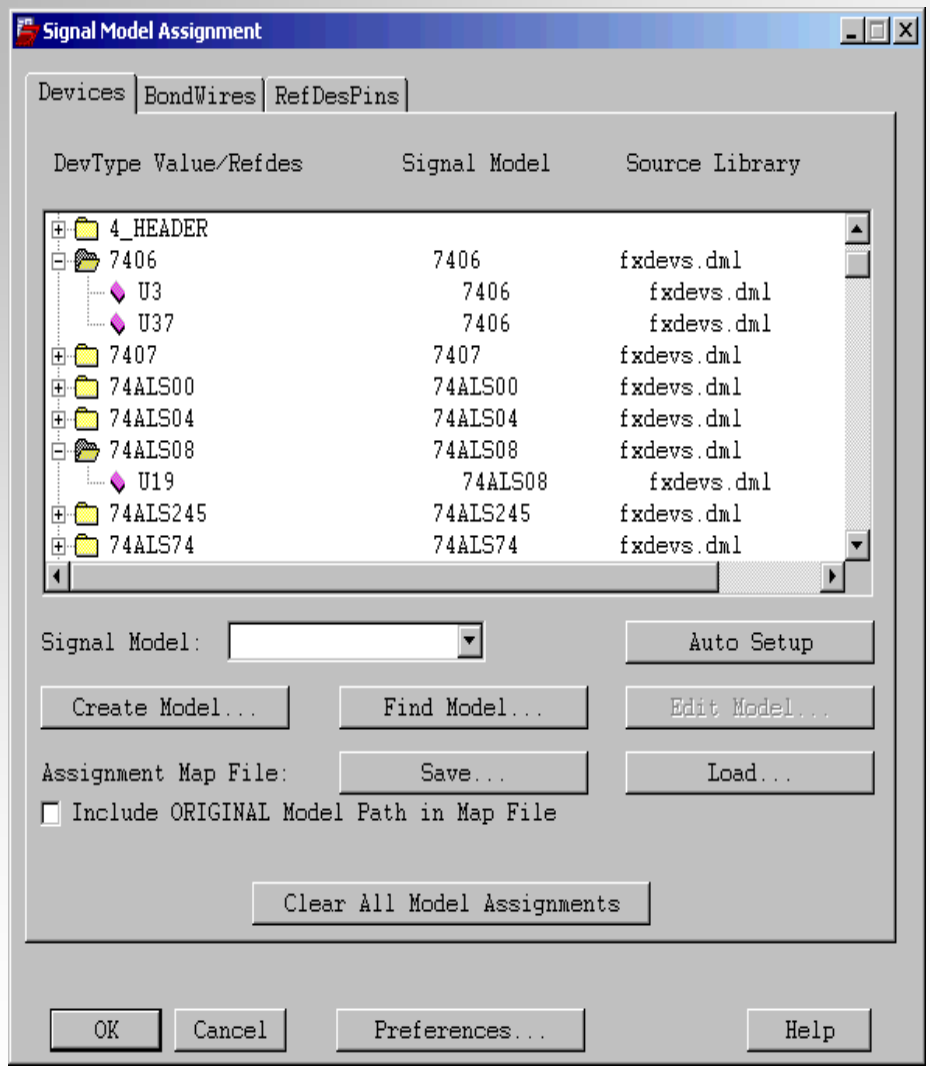


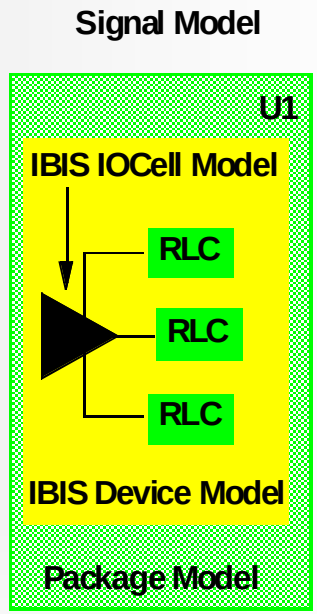
DC Voltages

SPECCTRAQuest SI Expert needs source voltages for terminators and capacitors to build an electrically correct circuit.



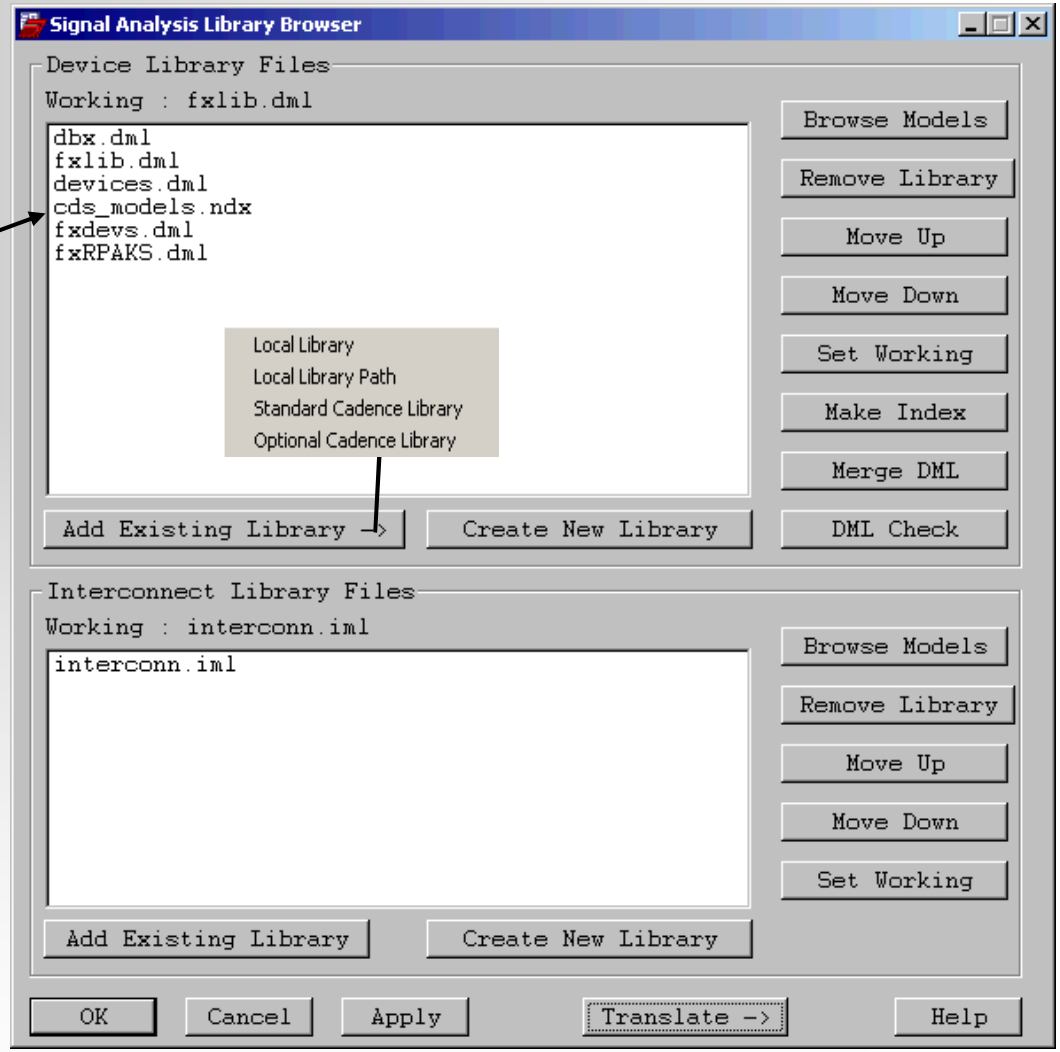
Signal Model Assignment Form





Translating and Adding Libraries

An Index file (.ndx) is a group of library files that have been merged and indexed together. You can use the models for simulation, but cannot modify the index file in any way.



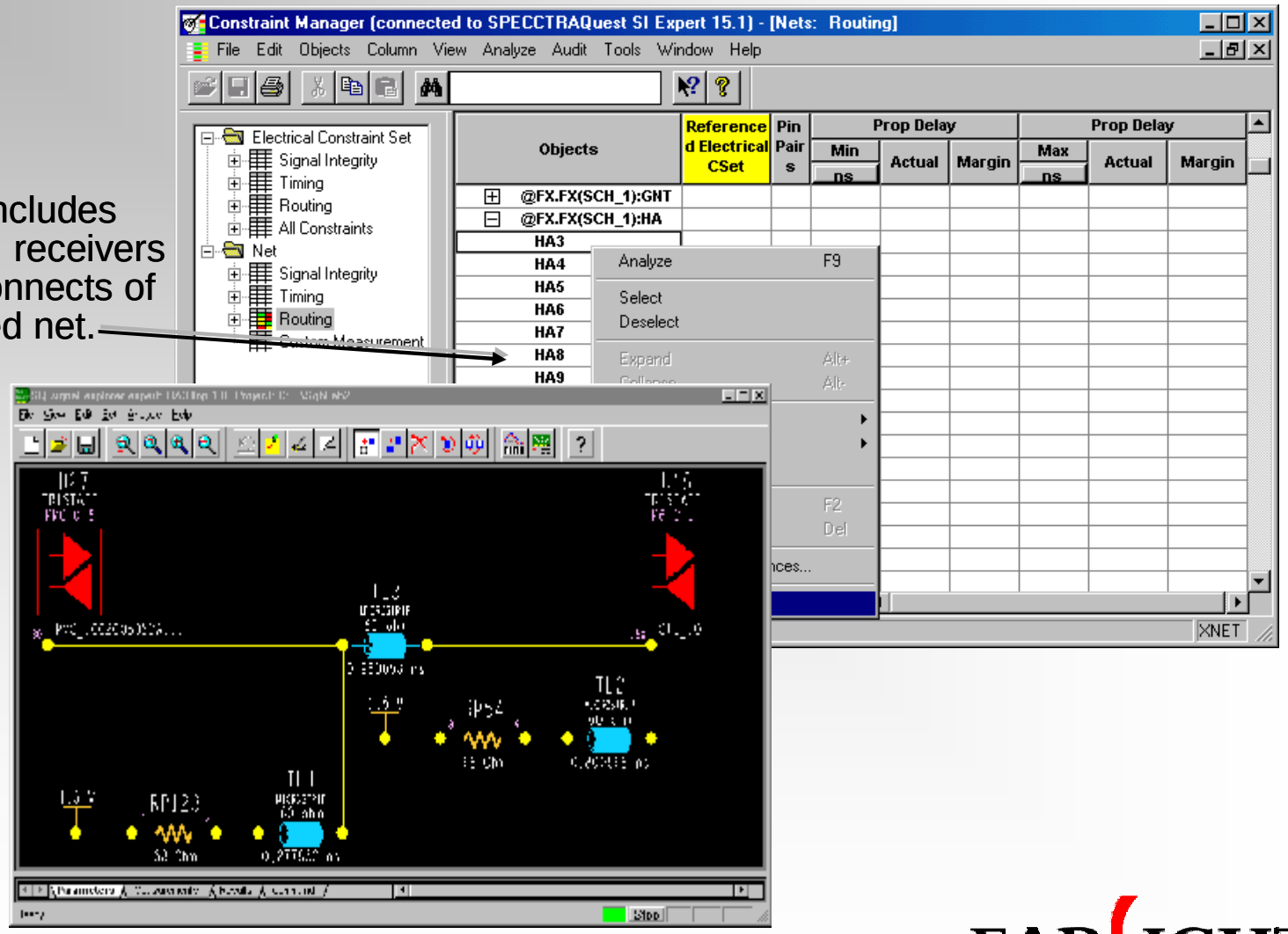
You can translate these types of signal models to SPECCTRAQuest format.

Ibis2signoise

quad2signoise

Pre-Route Template Extraction

The Xnet includes the drivers, receivers and interconnects of an extended net.



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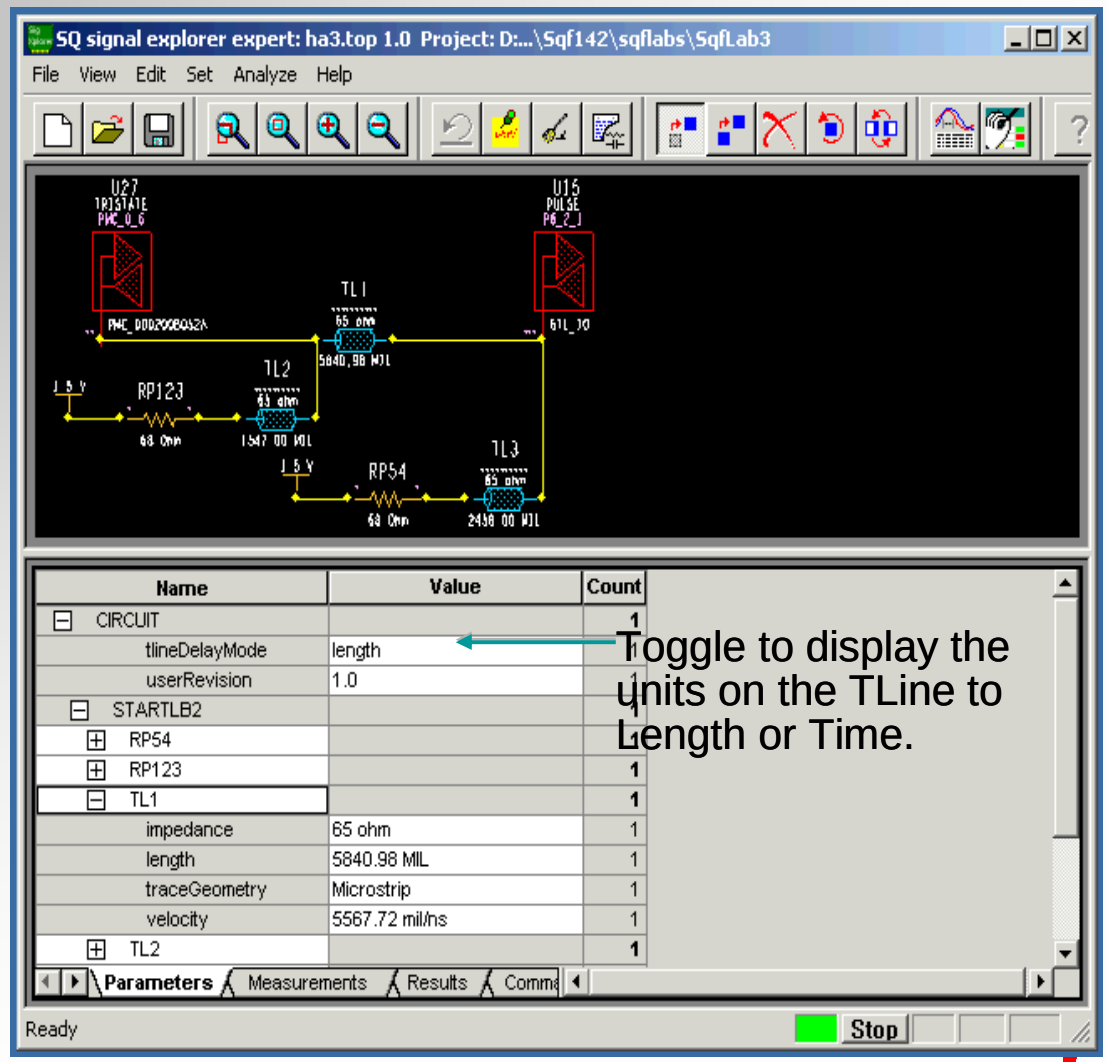
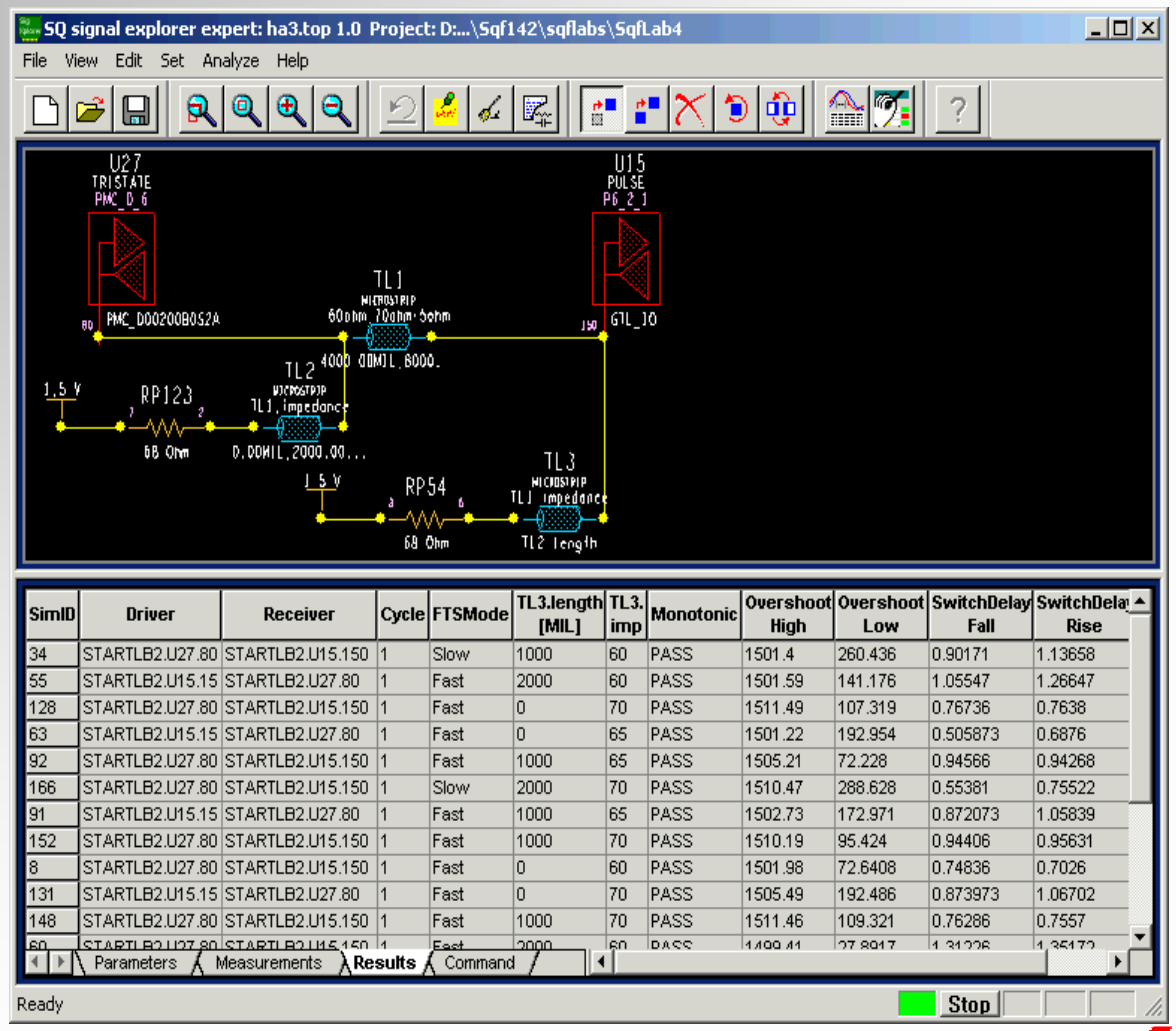
SQ Signal Explorer Expert Parameters Tab



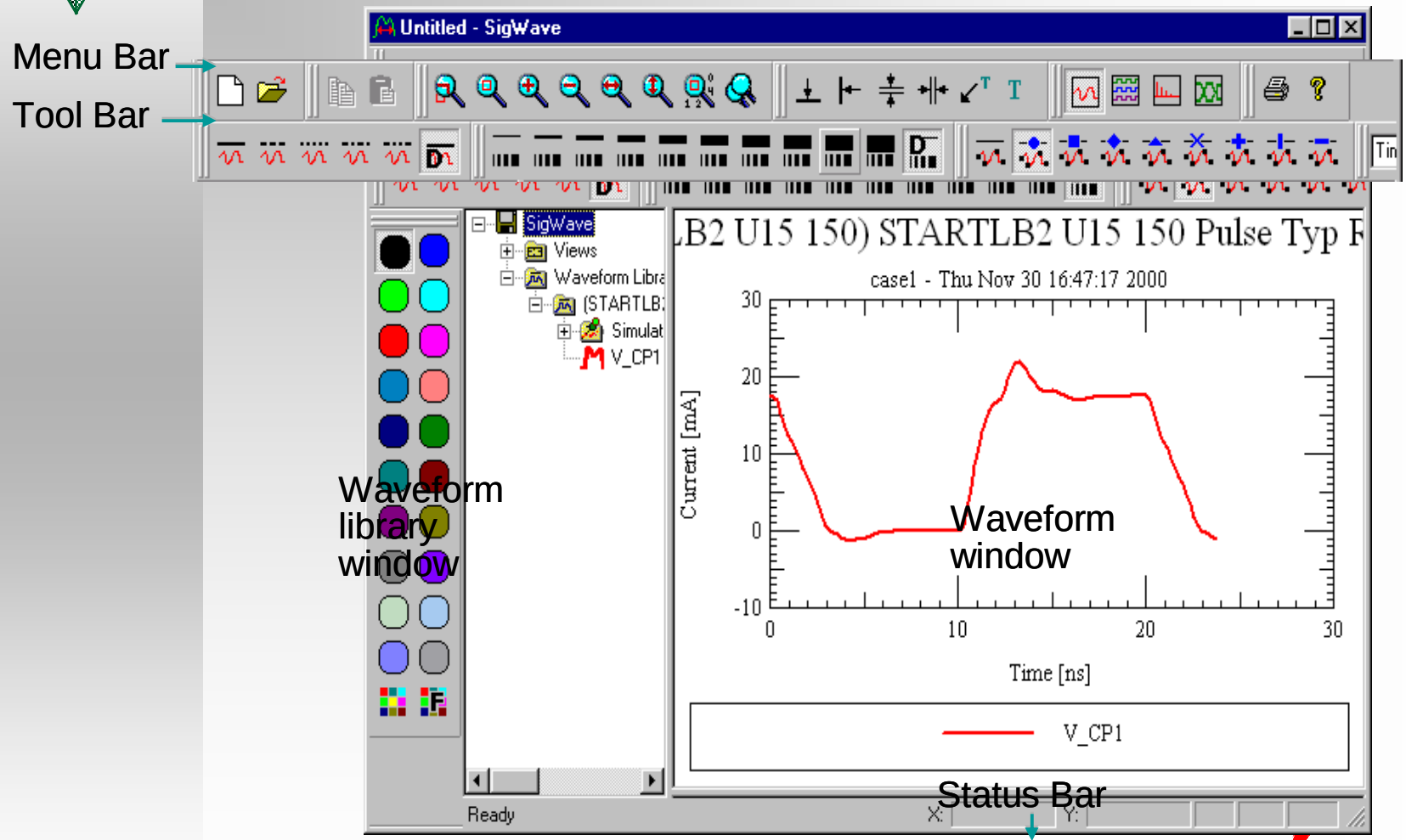
Toggle to display the units on the TLine to Length or Time.

SQ Signal Explorer Expert Results Tab



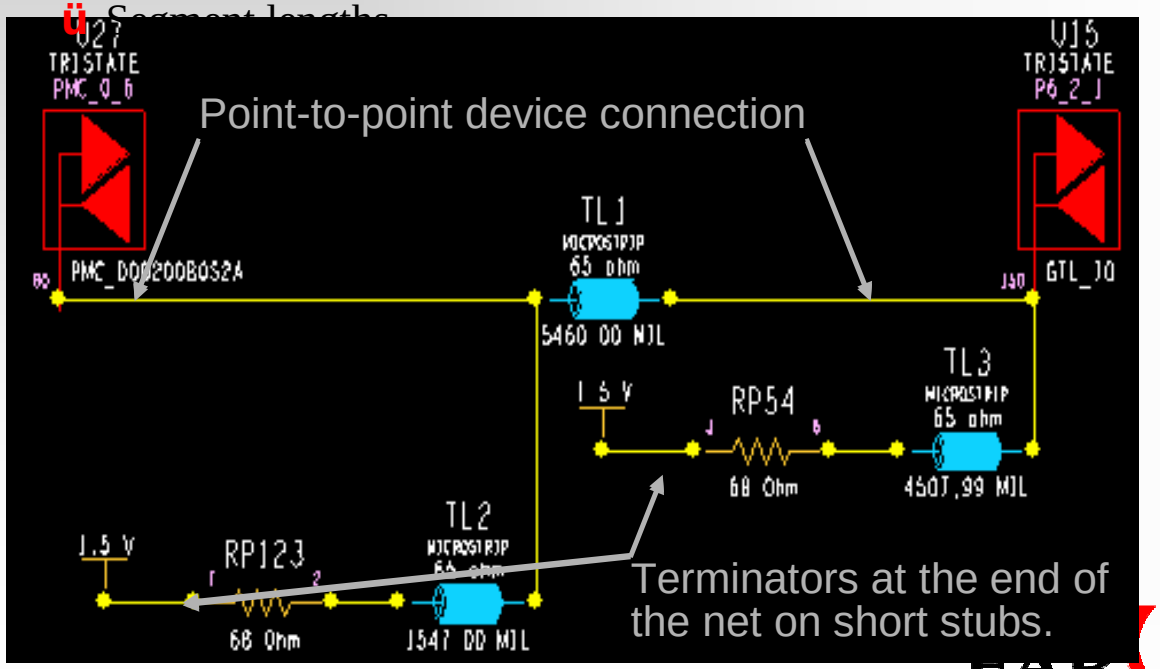
SimID	Driver	Receiver	Cycle	FTSMode	TL3.length [MIL]	TL3. imp	Monotonic	Overshoot High	Overshoot Low	SwitchDelay Fall	SwitchDela Rise
34	STARTLB2.U27.80	STARTLB2.U15.150	1	Slow	1000	60	PASS	1501.4	260.436	0.90171	1.13658
55	STARTLB2.U15.15	STARTLB2.U27.80	1	Fast	2000	60	PASS	1501.59	141.176	1.05547	1.26647
128	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	0	70	PASS	1511.49	107.319	0.76736	0.7638
63	STARTLB2.U15.15	STARTLB2.U27.80	1	Fast	0	65	PASS	1501.22	192.954	0.505873	0.6876
92	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	1000	65	PASS	1505.21	72.228	0.94566	0.94268
166	STARTLB2.U27.80	STARTLB2.U15.150	1	Slow	2000	70	PASS	1510.47	288.628	0.55381	0.75522
91	STARTLB2.U15.15	STARTLB2.U27.80	1	Fast	1000	65	PASS	1502.73	172.971	0.872073	1.05839
152	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	1000	70	PASS	1510.19	95.424	0.94406	0.95631
8	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	0	60	PASS	1501.98	72.6408	0.74836	0.7026
131	STARTLB2.U15.15	STARTLB2.U27.80	1	Fast	0	70	PASS	1505.49	192.486	0.873973	1.06702
148	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	1000	70	PASS	1511.46	109.321	0.76286	0.7557
60	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	2000	60	PASS	1499.41	27.8917	1.31226	1.35172

SigWave Current Waveforms



Solution Space Analysis Step 1

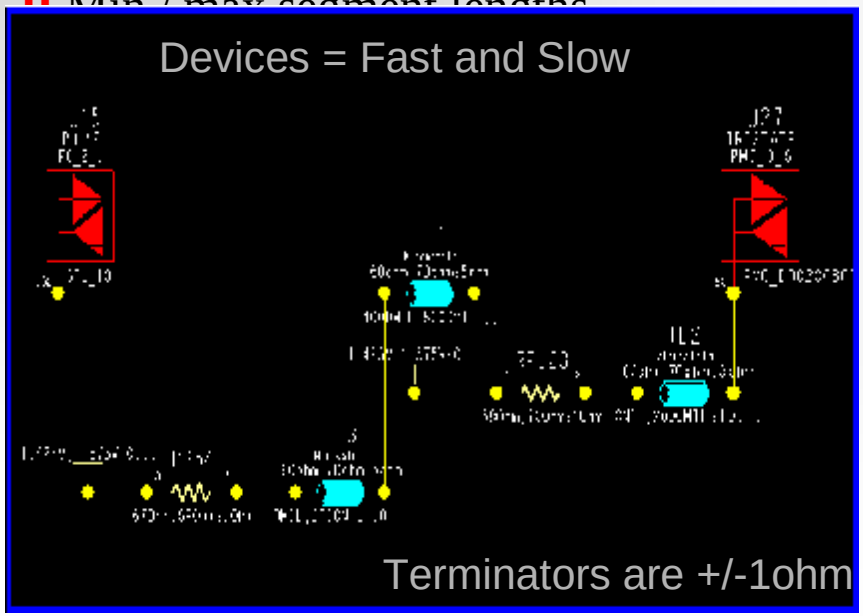
- Extract / create topology to be analyzed.
  - Pin ordering
  - Discrete devices
  - Rat-T positions (if any)
- Identify / enter nominal values for all parameters.
  - Board impedance
  - Trace velocity
  - Terminator value
  - Segment lengths



Solution Space Analysis Step 2

- Identify manufacturing variances that are to be included in the analysis.
  - Trace impedance (for example +/- 10%)
  - Trace velocity
  - Fast / slow components
  - Device values (ex. terminators)
  - Power supplies (if applicable)
- Identify initial ranges for "design rule" parameters.
  - Min / max segment lengths

1.5 volt supply is +/- 5%



Trace impedance is 65 ohms +/- 5 ohms.

Trace length varies for each TLine:
TL1: 4000 mils to 8000 mils,
TL2 and TL3: 0 mils to 2000 mils.

Solution Space Analysis Step 3

- Create a “master list” of all variables for analyses and their ranges.
- Identify “dependencies” between variables, based on how the design will be implemented.
  - Traces on the same layer have identical characteristics.
  - Resistors in the same RPAK match closely.
- D… to be ar…

Parameter	Min	Typ	Max	# Steps
P6 Speed	Fast		Slow	2
440FX_Speed	Fast		Slow	2
TL1 Impedance	60 ohms		70 ohms	2
TL1 Velocity	5400 mils/ns		6600 mils/ns	2
TL1 Length	4000 mils		8000 mils	2
TL2 Impedance		TL1 Impedance		1
TL2 Velocity		TL1 Velocity		1
TL2 Length	0 mils		2000 mils	2
TL3 Impedance		TL1 Impedance		1
TL3 Velocity		TL1 Velocity		1
TL3 Length	0 mils		2000 mils	2
RP A Impedance	67 ohms		69 ohms	2
RP B Impedance	67 ohms		69 ohms	2
Total Combinations				**512**

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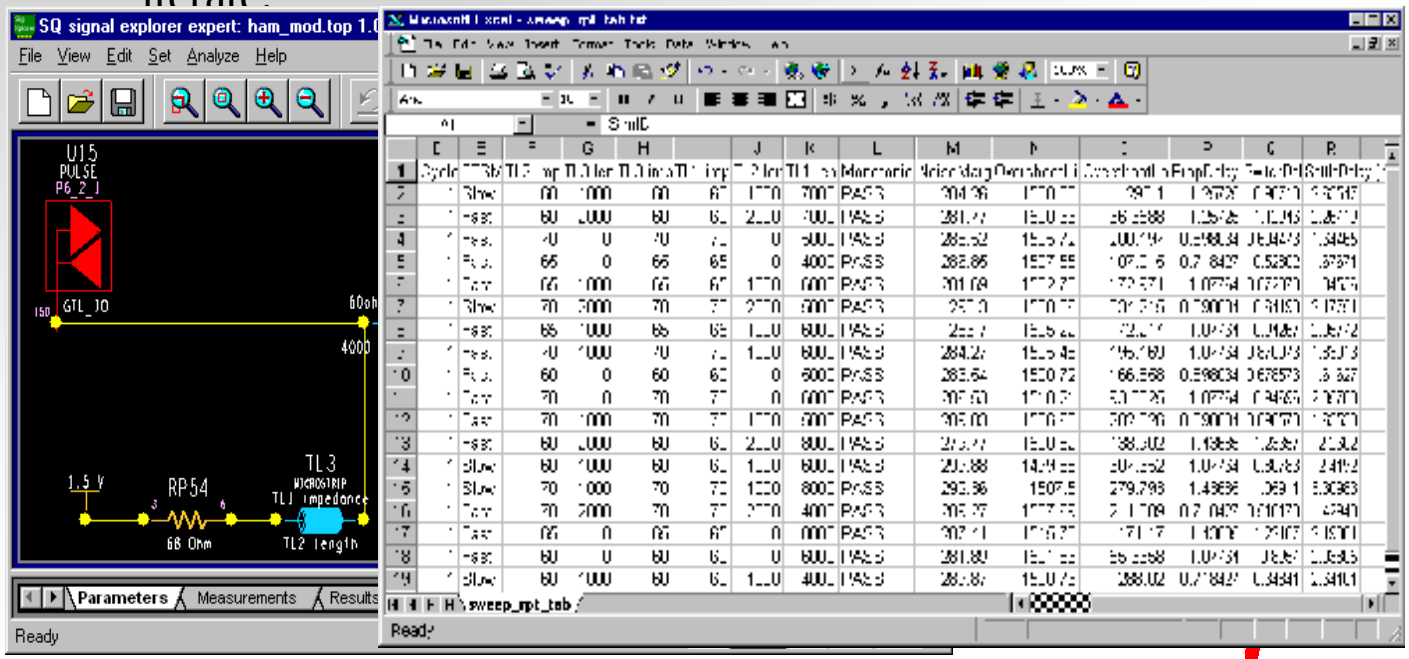
Solution Space Analysis Step 4

- Run simulations and gather results.
  - SigXp “tabbed” report format is designed to import easily into Microsoft Excel and Access.
- Evaluate results and identify “cases” (combinations of variables) that cause topology to fail (not meet design goals).
- Simulate individual cases, analyze, correct design if needed, and iterate.



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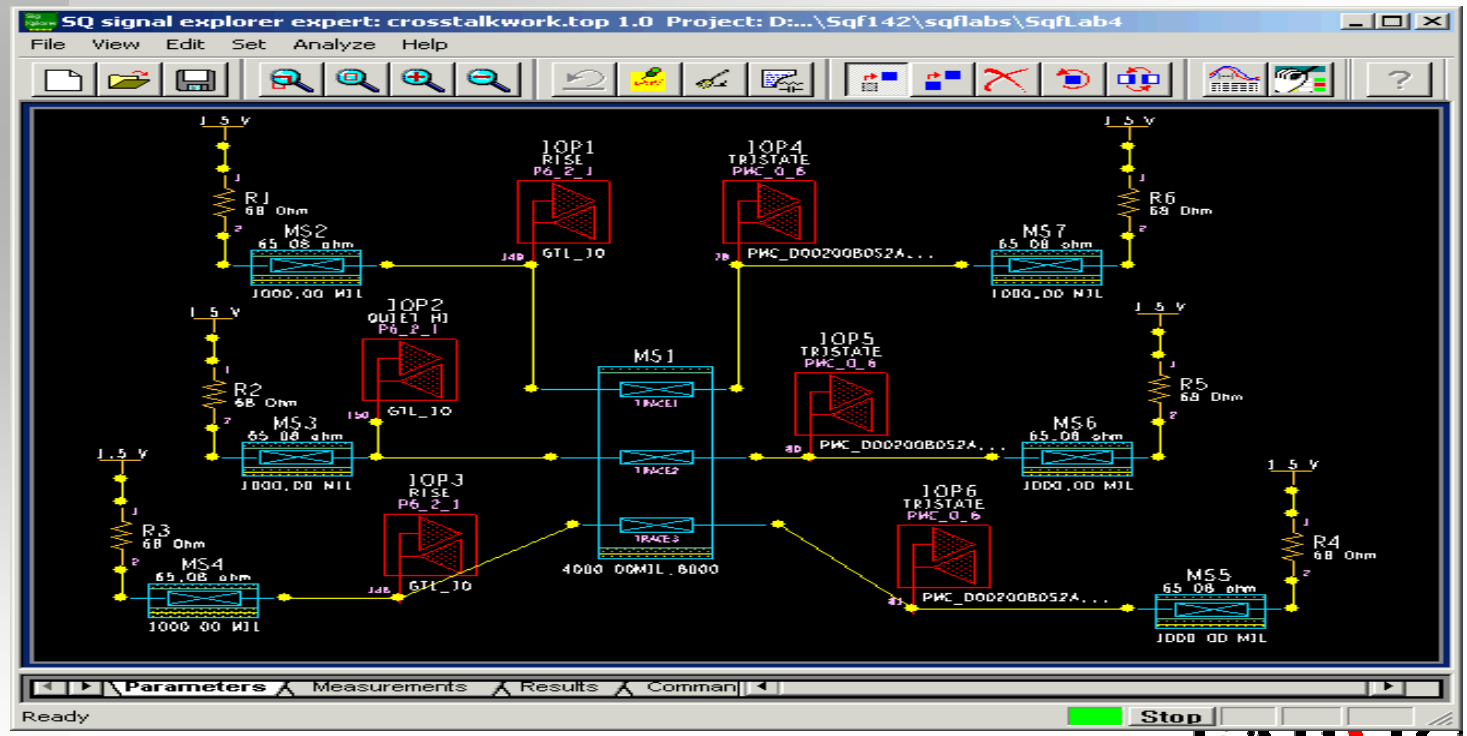
Solution Space Analysis Step 5

- The solution found thus far is a single-line solution.
- Crosstalk timing shifts must be within crosstalk budget.
- Single-line topology is modified to model coupling where appropriate.
- Different line width / spacing rules are evaluated for timing



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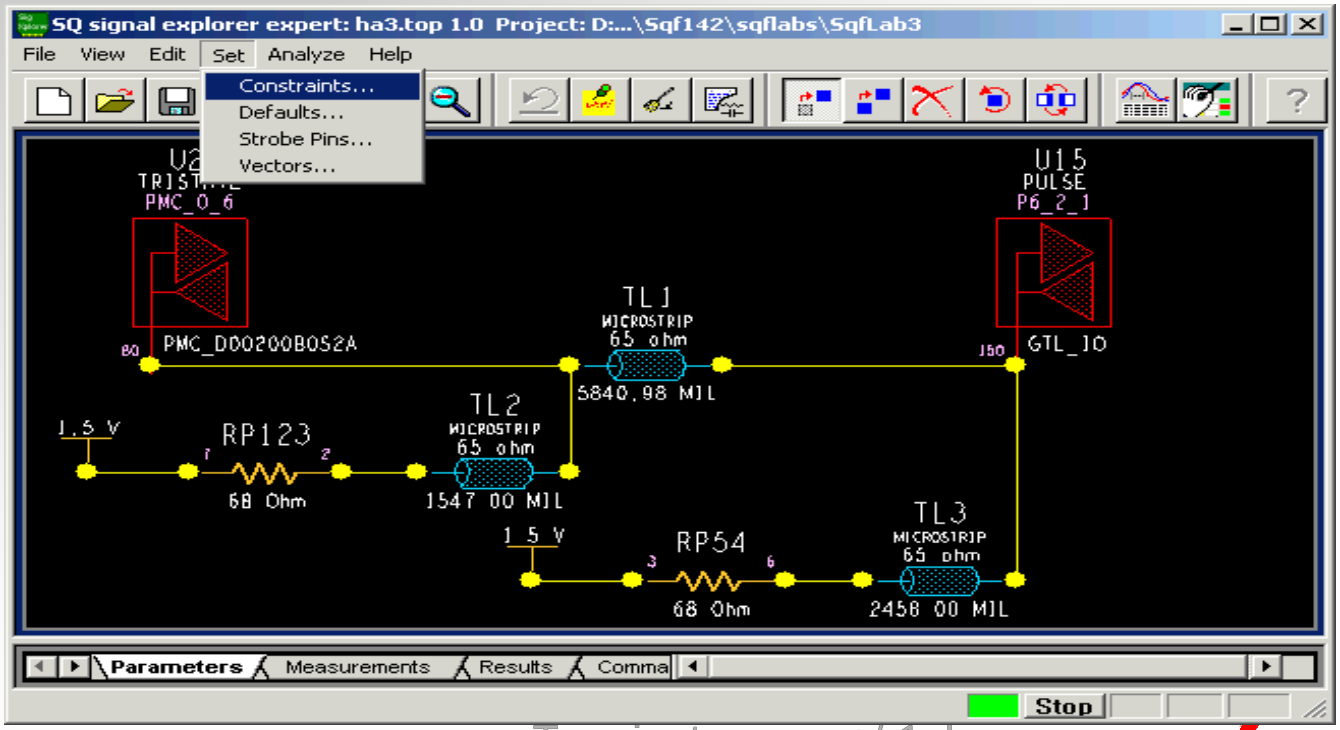
Solution Space Analysis Step 6

- Create final topology template from analysis results:
  - Segment min / max lengths
  - Parallelism rules
- Some variances should not be included in the final topology template:



Terminators are +/-1ohm

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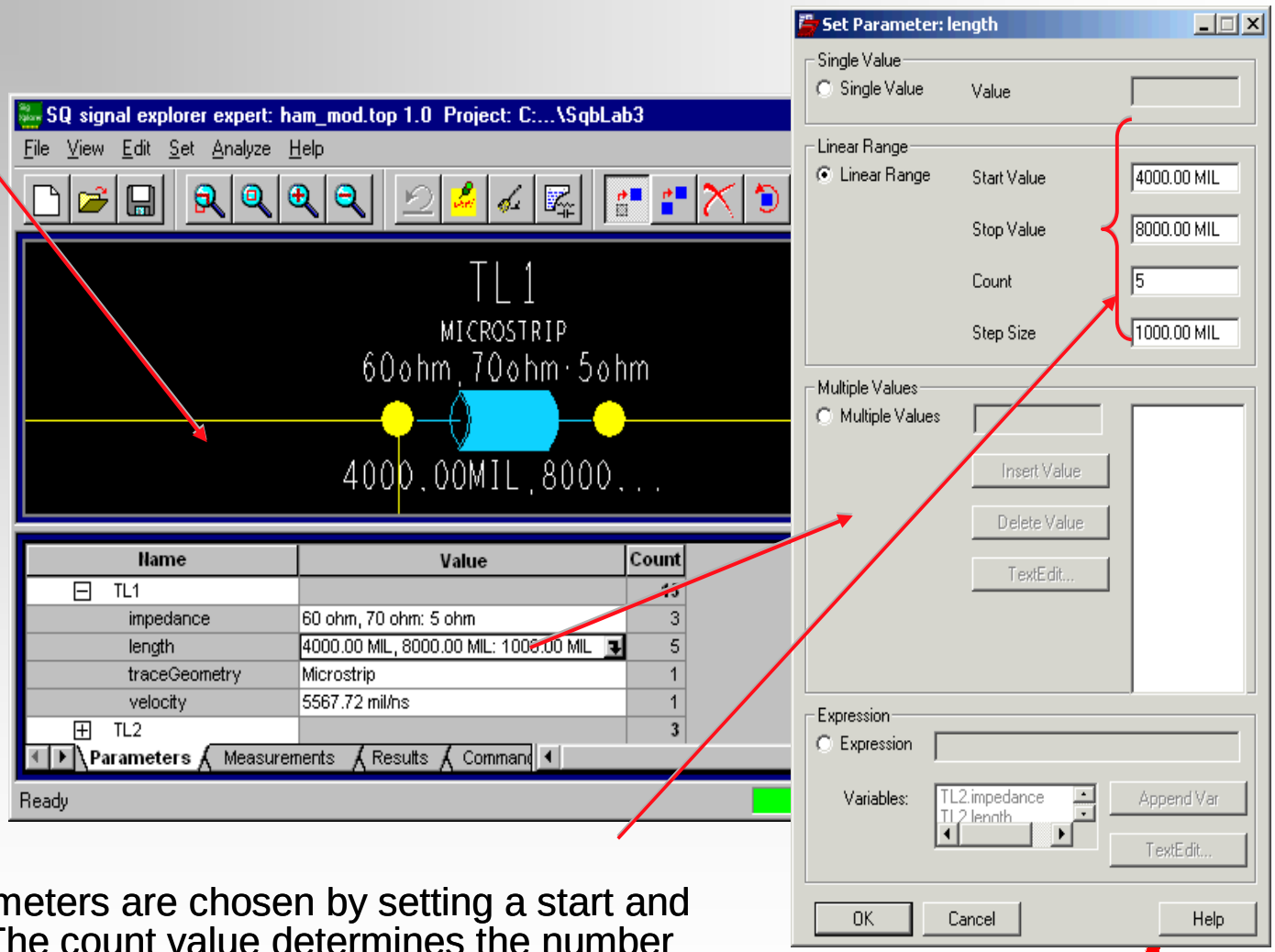
Parametric Sweeps

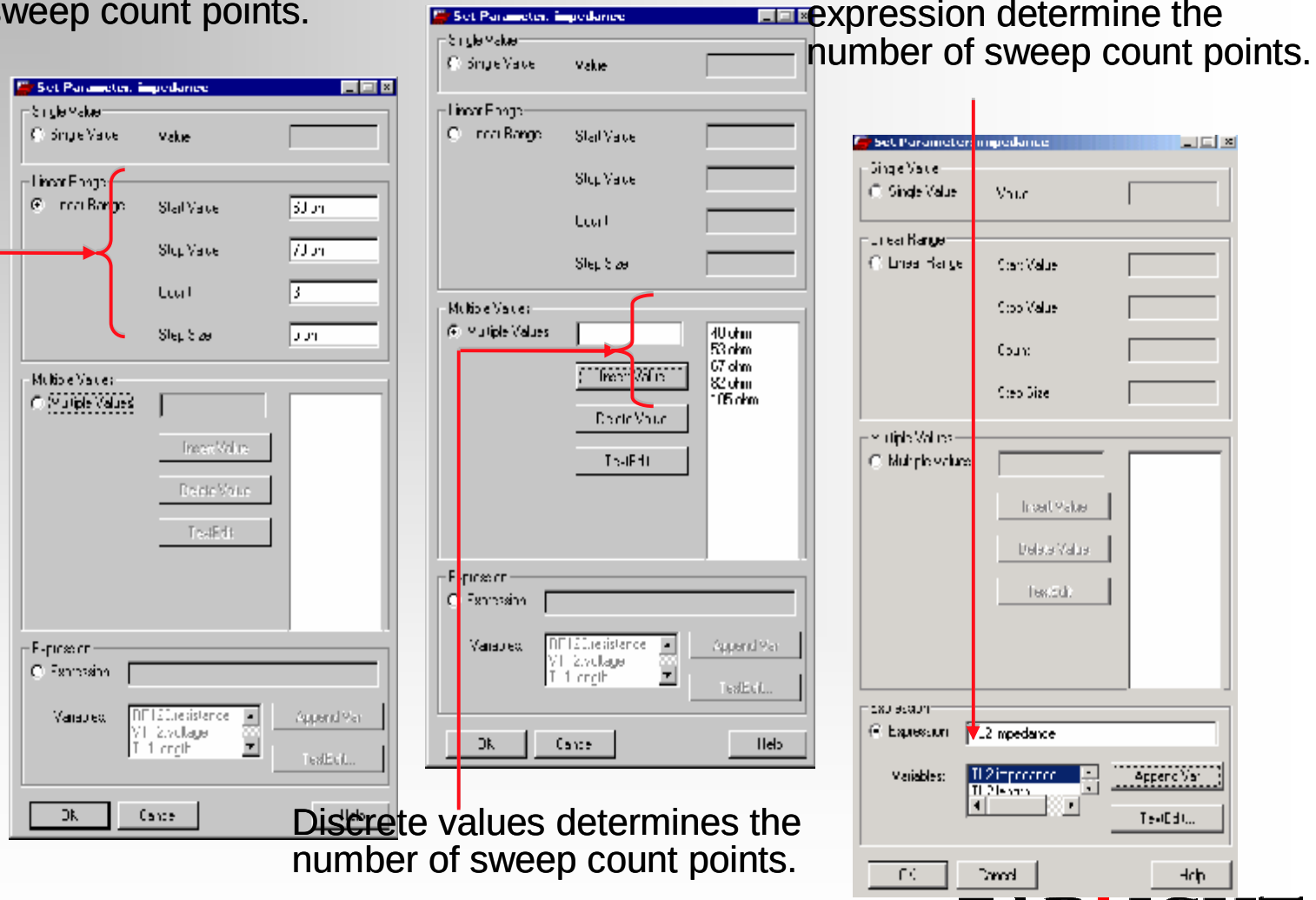


Sweep parameters are chosen by setting a start and stop value. The count value determines the number of sweep count points.

Setting Sweep Parameters

Count value determines the number of sweep count points.

Expression listed and other parameters used in the expression determine the number of sweep count points.



Discrete values determines the number of sweep count points.

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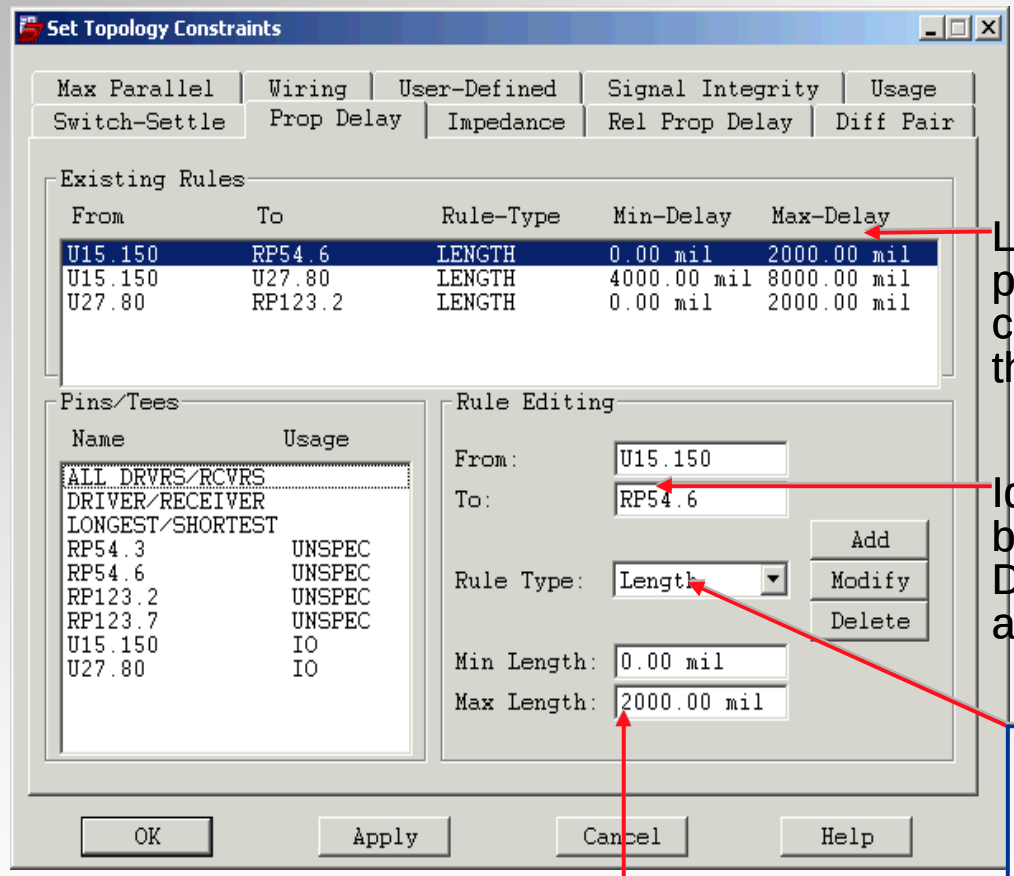
Assigning Prop Delay Constraints



List the Pin or Pin-Tee pairs that have delay constraints assigned in the current topology.

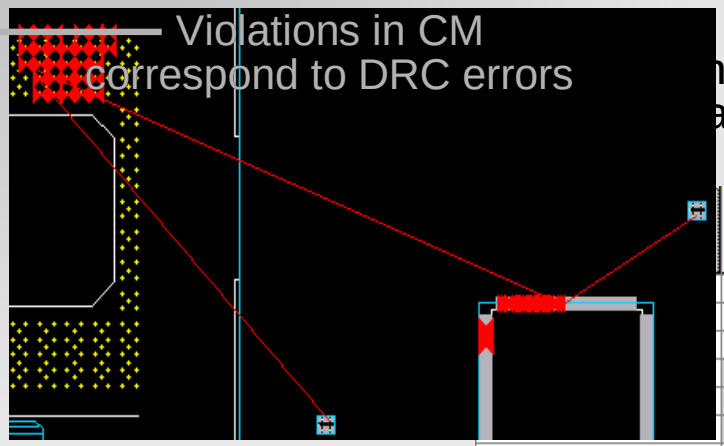
Identify the desired points between which Prop Delay constraint is to be applied.

Delay
Length
% Manhattan

Components are listed with their pinuse values.

Identify the desired min and max delay acceptable for this pair.

Template Applications and Constraint-Driven Placement



Violations in CM correspond to DRC errors

nstraint alues

Actual manhattan routing distance

Worst case bubbles to the top

	Referenced Electrical CSet	Pin Pairs	Prop Delay Min ns	Prop Delay Actual	Prop Delay Margin	Prop Delay Max ns	Prop Delay Actual	Prop Delay Margin
	HA3							-17607 MIL
	HA3							-2508 MIL
			0 MIL	4508 MIL	4508 MIL	2000 MIL	4508 MIL	-2508 MIL
			4000 MIL			8000 MIL	5460 MIL	2540 MIL
			0 MIL			2000 MIL	1547 MIL	453 MIL
HA4	HA3							-17607 MIL
U15.149:RP48.4			0 MIL	19607 MIL	19607 MIL	2000 MIL	19607 MIL	-17607 MIL
U15.149:U27.78			4000 MIL			8000 MIL	5600 MIL	2400 MIL
U27.78:RP123.3			0 MIL			2000 MIL	1538 MIL	462 MIL
HA5	HA3							-8557 MIL
U15.140:RP124.3			0 MIL	10557 MIL	10557 MIL	2000 MIL	10557 MIL	-8557 MIL
U15.140:U27.83			4000 MIL			8000 MIL	5301 MIL	2699 MIL
U27.83:RP60.6			0 MIL	8735 MIL	8735 MIL	2000 MIL	8735 MIL	-6735 MIL
HA6	HA3							-10422 MIL
U15.148:RP55.1			0 MIL	12422 MIL	12422 MIL	2000 MIL	12422 MIL	-10422 MIL
U15.148:U27.77			4000 MIL			8000 MIL	5720 MIL	2280 MIL
U27.77:RP123.4			0 MIL			2000 MIL	1549 MIL	451 MIL

Wiring | Impedance | Min/Max Propagation Dela

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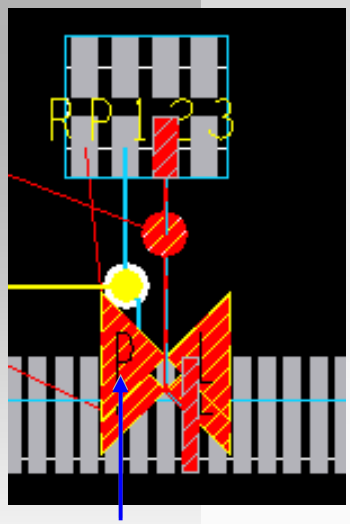
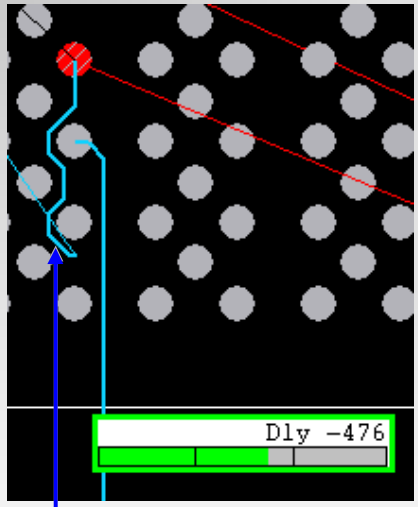
Constraint-Driven Routing

Bubble: Off



The spacing rule violation flagged off by DRC markers

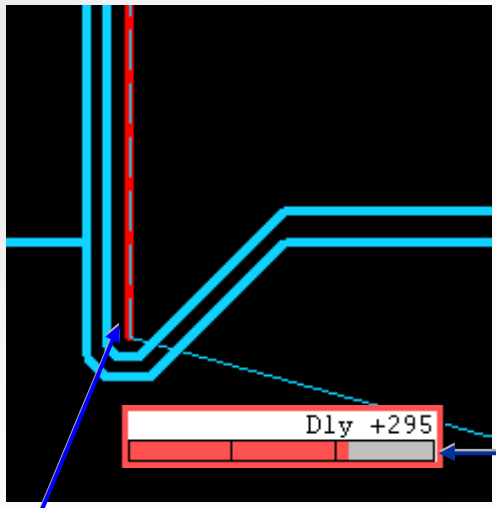
Bubble: Hug Preferred



The etch that is routed hugs the object to avoid DRC violation.

Dynamic timing meter highlights high-speed timing constraint violation.

Bubble: Shove Preferred



The etch that is routed pushes the existing etch to resolve DRC violation.

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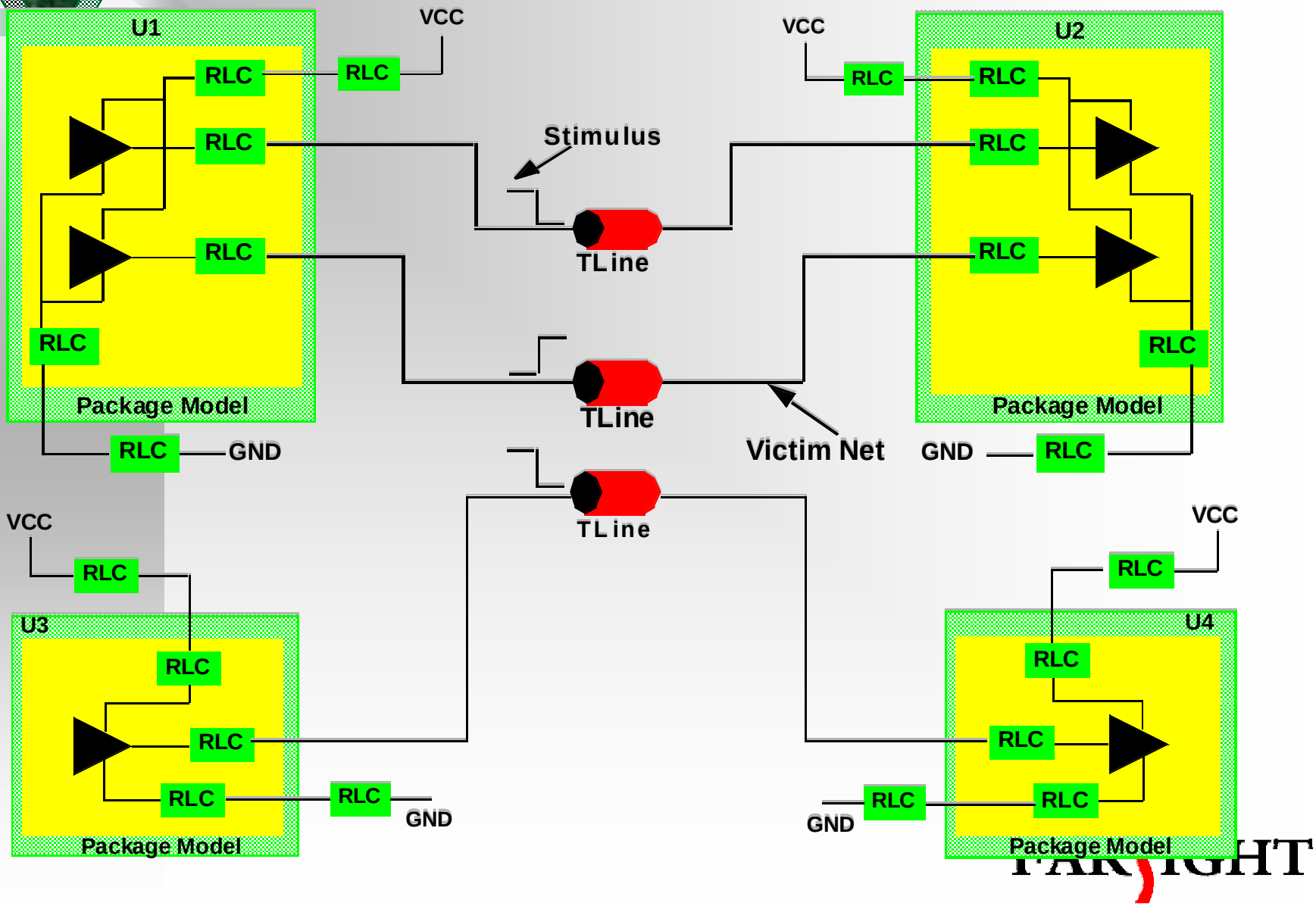
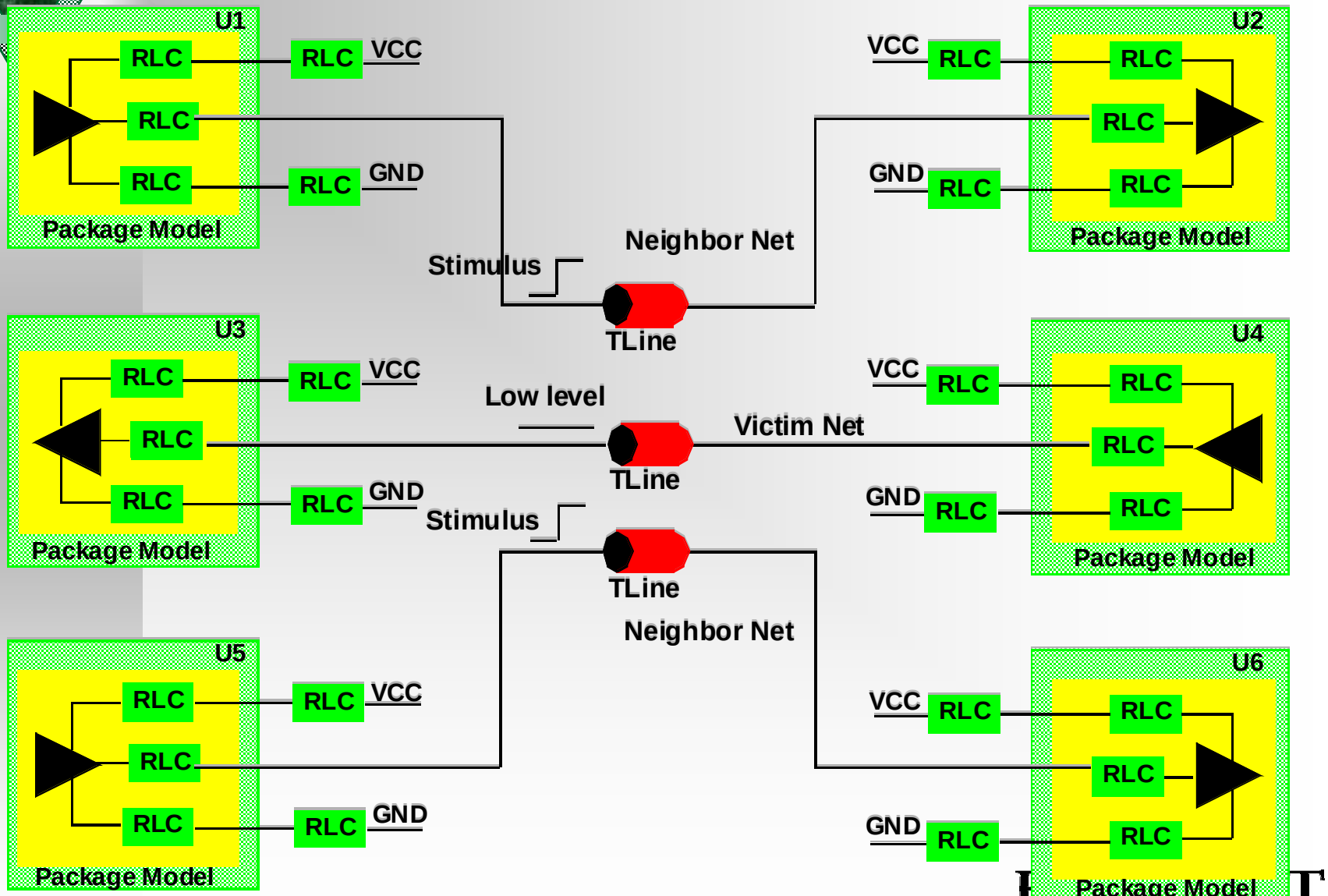
Post-Route DRC and Analysis



Crosstalk Simulation



Simultaneous Switching Noise Report

Results from a SSN simulation:

```
**********************************************************************************
Simultaneous Switching Noise (mV) for XNet `2 COMPLETE HA4` (Typ FTSMode)
**********************************************************************************
Drvr                Net             PowerBus   SSNRise   GroundBus   SSNFall
-----------------   -------------   --------   -------   ---------   -------
COMPLETE U15 149    COMPLETE HA4    pwrgtl     0         gndbus      51.54
----------------------------------------------------------------------------------

**********************************************************************
Driver I/O Characteristics (Typ FTSMode) RiseSlew/FallSlew in (mV/ns)
**********************************************************************
Drvr                IOModel   Volmax   Vohmin    RiseSlew   FallSlew
-----------------   -------   ------   -------   --------   --------
COMPLETE U15 149    GTL_IO    400 mV   3000 mV   271        284
----------------------------------------------------------------------

**********************************************************
Load I/O Characteristics
**********************************************************
Rcvr               IOModel                  Vilmax   Vihmin
---------------    ---------------------    ------   -------
COMPLETE U27 78    PMC_D00200B0S2AZZGHE     800 mV   1200 mV
----------------------------------------------------------

**************************************************************
Pulse Data Per Xnet
**************************************************************
XNet               PulseFreq   PulseDutyCycle   PulseCycleCount
--------------     ---------   --------------   ---------------
2 COMPLETE HA4     66MHz       0.5              1
--------------------------------------------------------------

**********************************************************************
```

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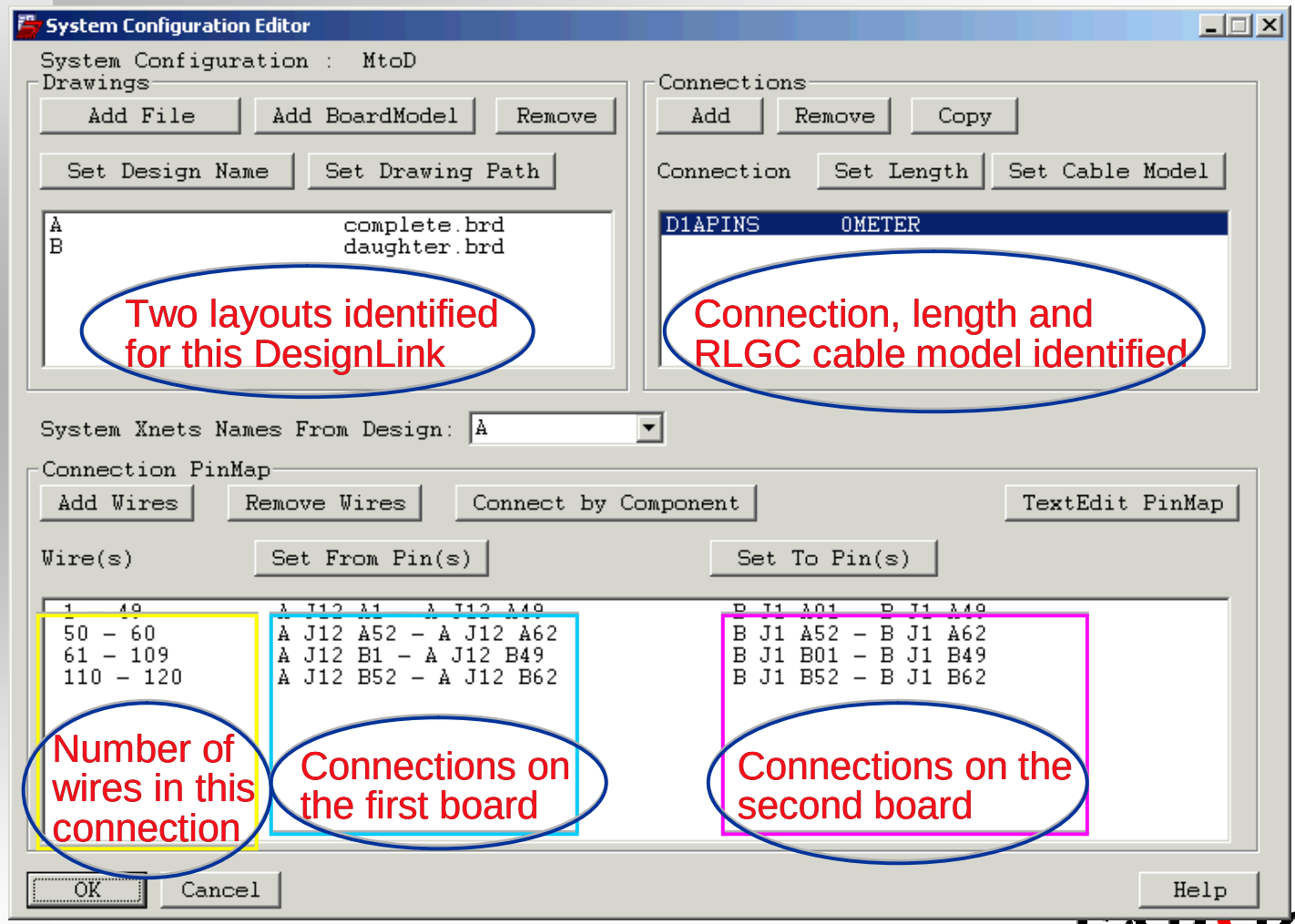
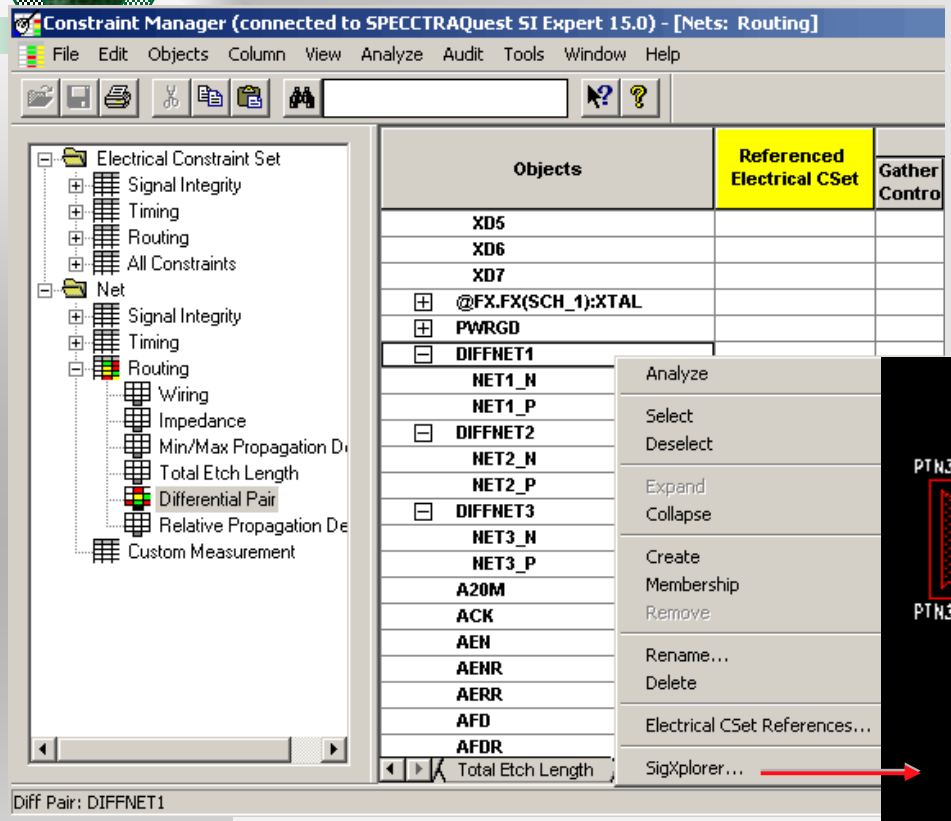
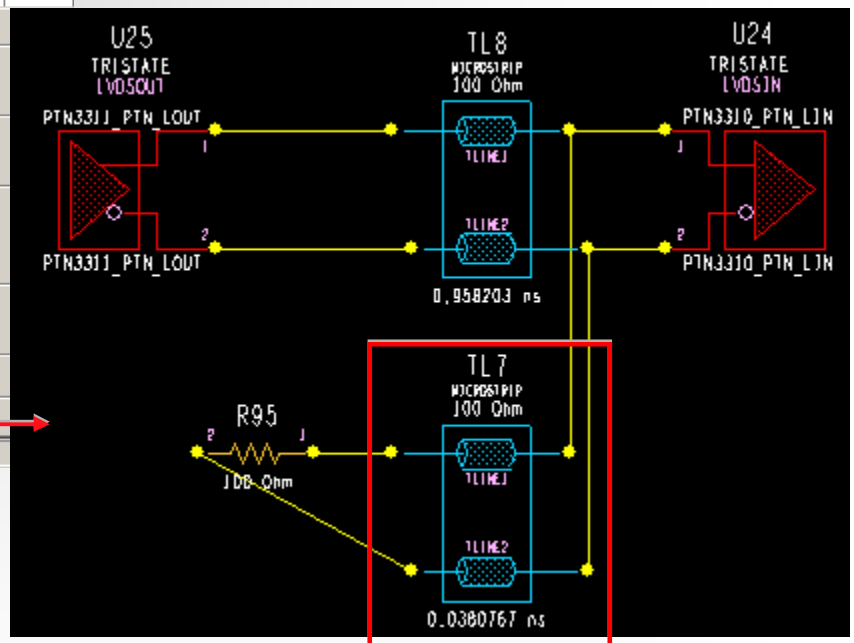
System-Level Analysis



Differential Pair Design Exploration





Extracted Ideal TlineCoupled model

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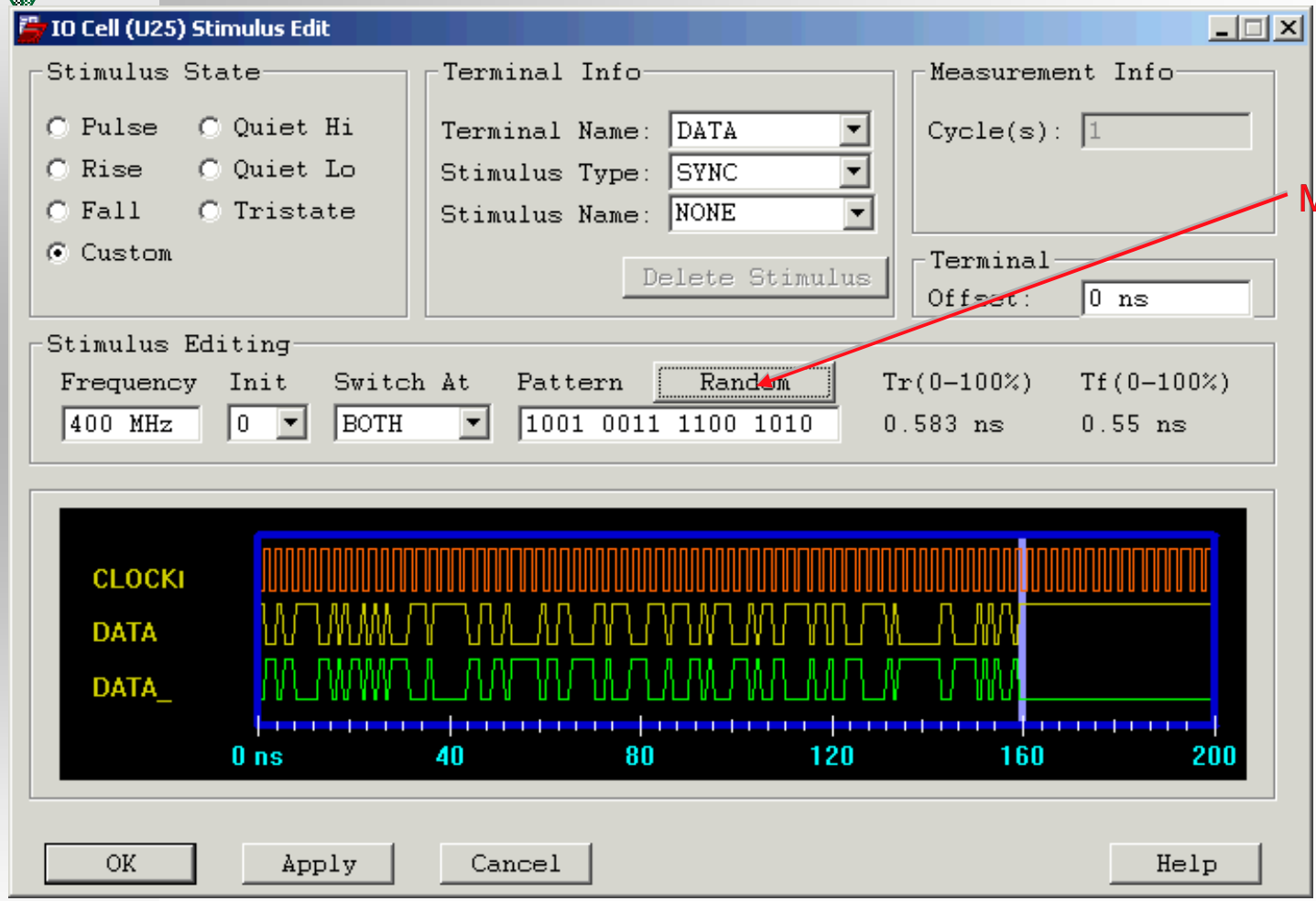
Custom Stimulus to Analyze Differential Pair Topology



Maximum of 1024 bits

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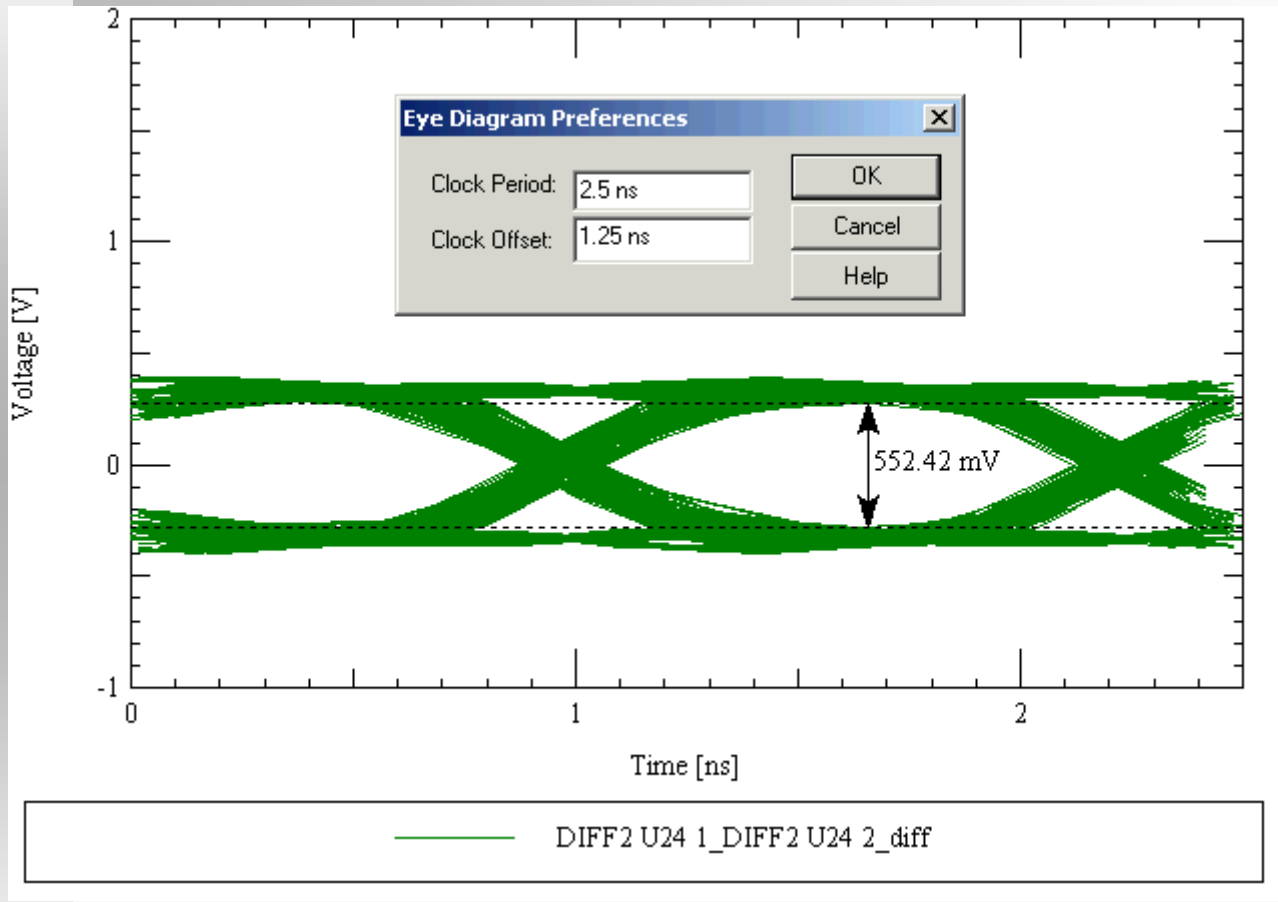
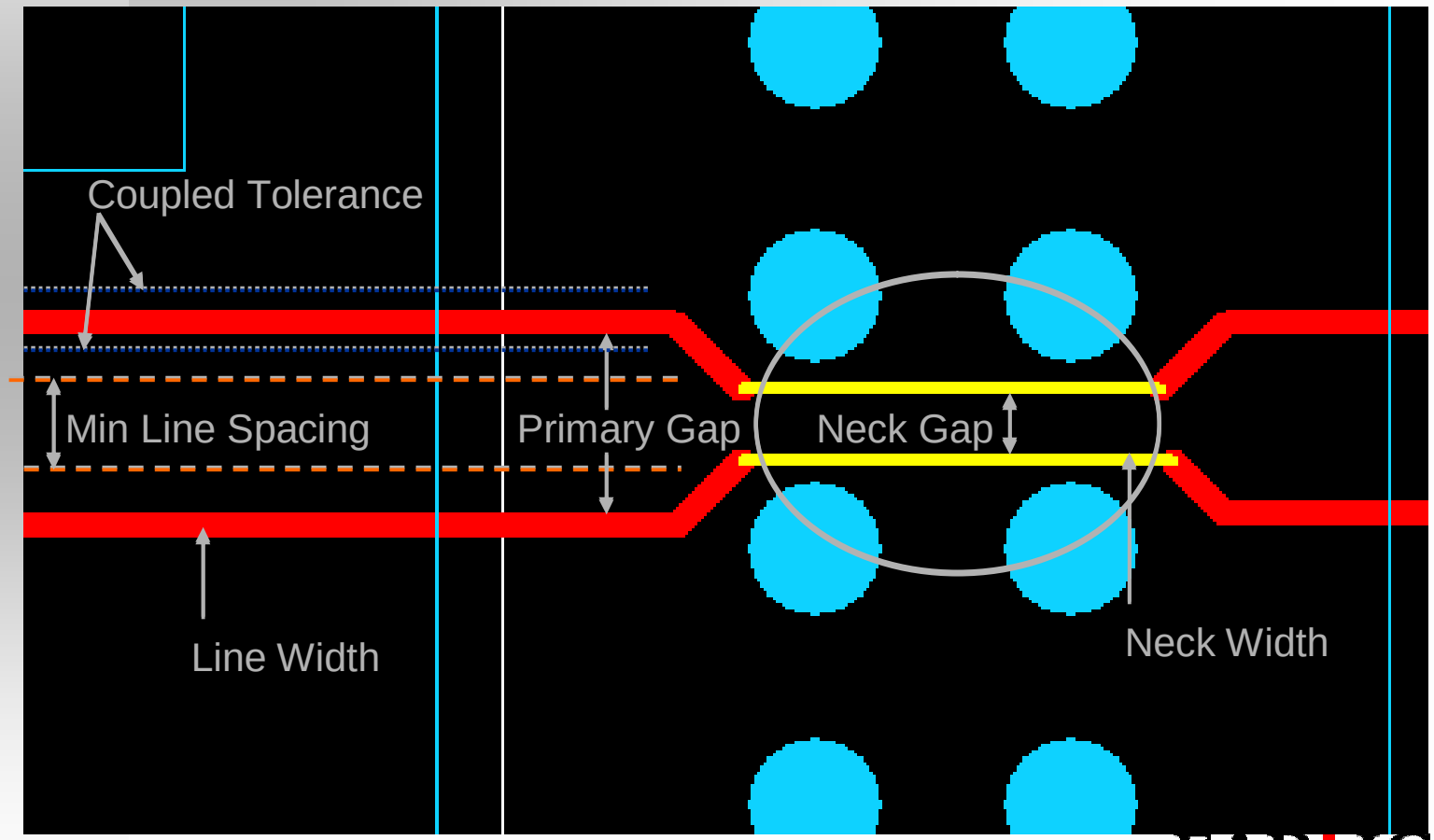
Differential Pair Topology Analysis



Gap and Line Width

From the SPECCTRAQuest SI Expert menu, select Route—Connect command.



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华清远见CADENCE相关课程

- 初级班(三天)
- 1. Concept HDL 原理图设计
- 2. Allegro PCB设计
- 3. Librarian Expert 库管理

- 高级班(三天)
- Day 1: Basic theories in high-speed PCB design
- Pre-Placement
- Extracting and Simulating Topologies
- Day 2: Determining and Adding Constraints
- Template Applications and Constraint-Driven Placement
- Day 3: Constraint-Driven Routing
- Post-Route DRC and Analysis
- Differential Pair Design Exploration

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让我们一起讨论！

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谢谢！