



SPECCTRAQuest Foundations

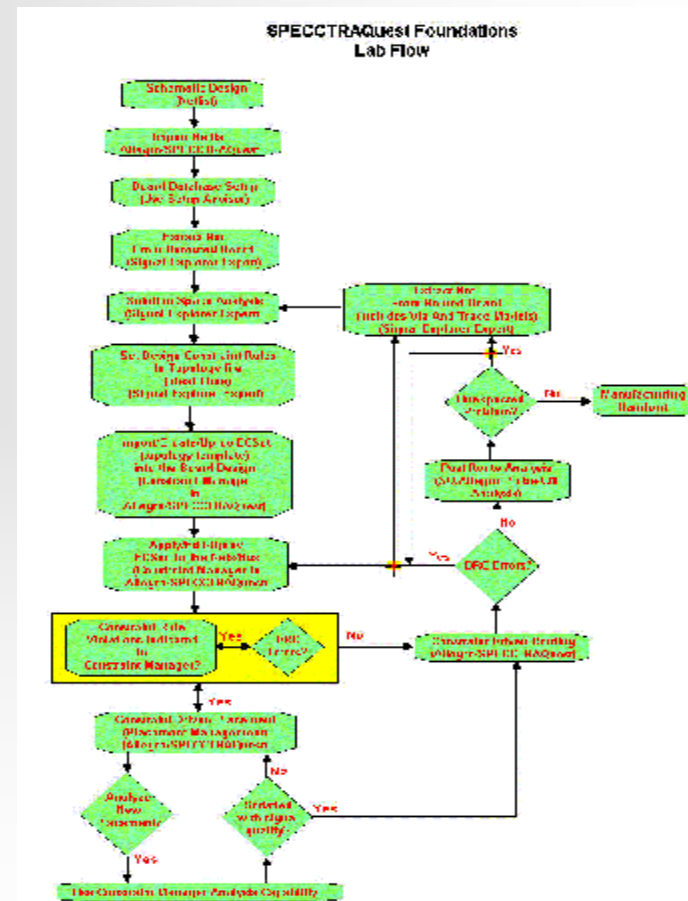
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The SPECCTRAQuest Design Flow

The SPECCTRAQuest Design Flow consists of the following six steps:

- Pre-Placement
- Solution Space Analysis
- Constraint-Driven Floorplanning
- Constraint-Driven Routing
- Post-Route DRC
- Post-Route Analysis

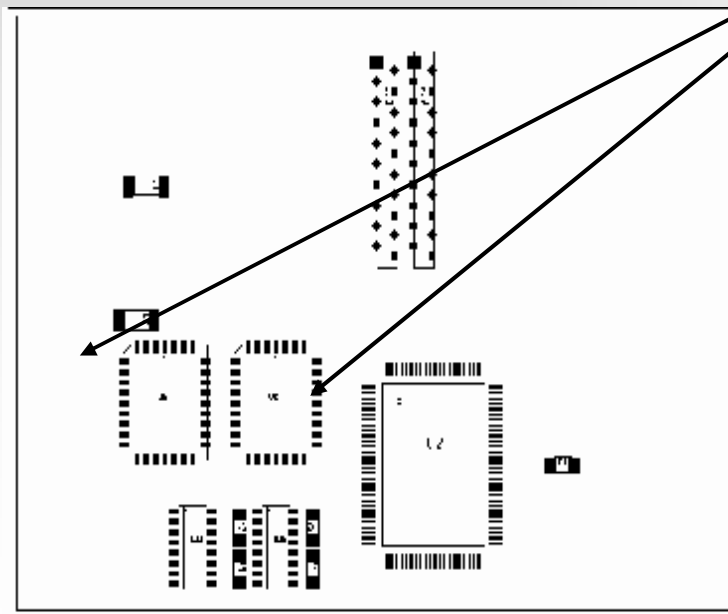


Design Flow: Pre-Placement

Standard form factors, mechanical restrictions, and standard practices often predefine locations of critical components.

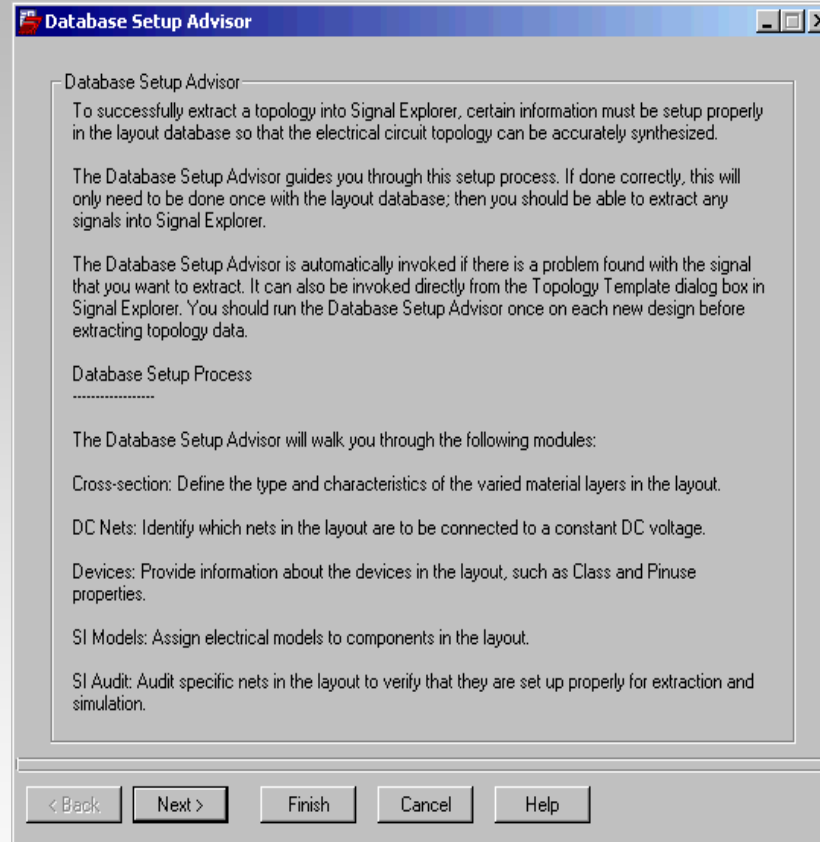
Electrical design must start with these requirements, or present a strong case why things should be changed.

Pre-placed design is usually created by the CAD group as a starting point for design.



Chip set placement predetermined

Database Setup Advisor



- Ø The first screen of the Database Setup Advisor.
- Ø Explains the use of Database Setup Advisor.
- Ø Describes the steps you must take to set up the database correctly.
- Ø “Set up Right, Set up Once”.

Defining the Layout Cross-Section

Layout Cross Section

Cross Section

| | Subclass Name | Type | Material | Thickness (MIL) | Conductivity (mho/cm) | Dielectric Constant | Loss Tangent | Negative Artwork | Shield | Width (MIL) | Impedance (ohm) |
|---|---------------|------------|----------|-----------------|-----------------------|---------------------|--------------|-------------------------------------|-------------------------------------|-------------|-----------------|
| 1 | | SURFACE | AIR | | | | | | | | |
| 2 | TOP | CONDUCTOR | COPPER | 1.2 | 595900 | 1 | 0 | <input type="checkbox"/> | | 5 | 65.777 |
| 3 | | DIELECTRIC | FR-4 | 5 | 0 | 4.500000 | 0 | | | | |
| 4 | INTERNAL1 | PLANE | COPPER | 1.2 | 595900 | | | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | | |
| 5 | | DIELECTRIC | FR-4 | 14 | 0 | 4.500000 | 0 | | | | |
| 6 | INTERNAL2 | PLANE | COPPER | 1.2 | 595900 | | | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | | |
| 7 | | DIELECTRIC | FR-4 | 5 | 0 | 4.500000 | 0 | | | | |
| 8 | BOTTOM | CONDUCTOR | COPPER | 1.2 | 595900 | 1 | 0 | <input type="checkbox"/> | | 5 | 65.777 |
| 9 | | SURFACE | AIR | | | | | | | | |

Designates the currently selected layer as a shield layer. The shield layer prevents the electrical signals from the two adjacent layers from interacting with each other.

Activate Differential Mode
Layout Cross-Section Editor

Total Thickness: 28.8 MIL

Stripline Layer Dielectric: [Determined Automatically]

Dielectric Constant: []

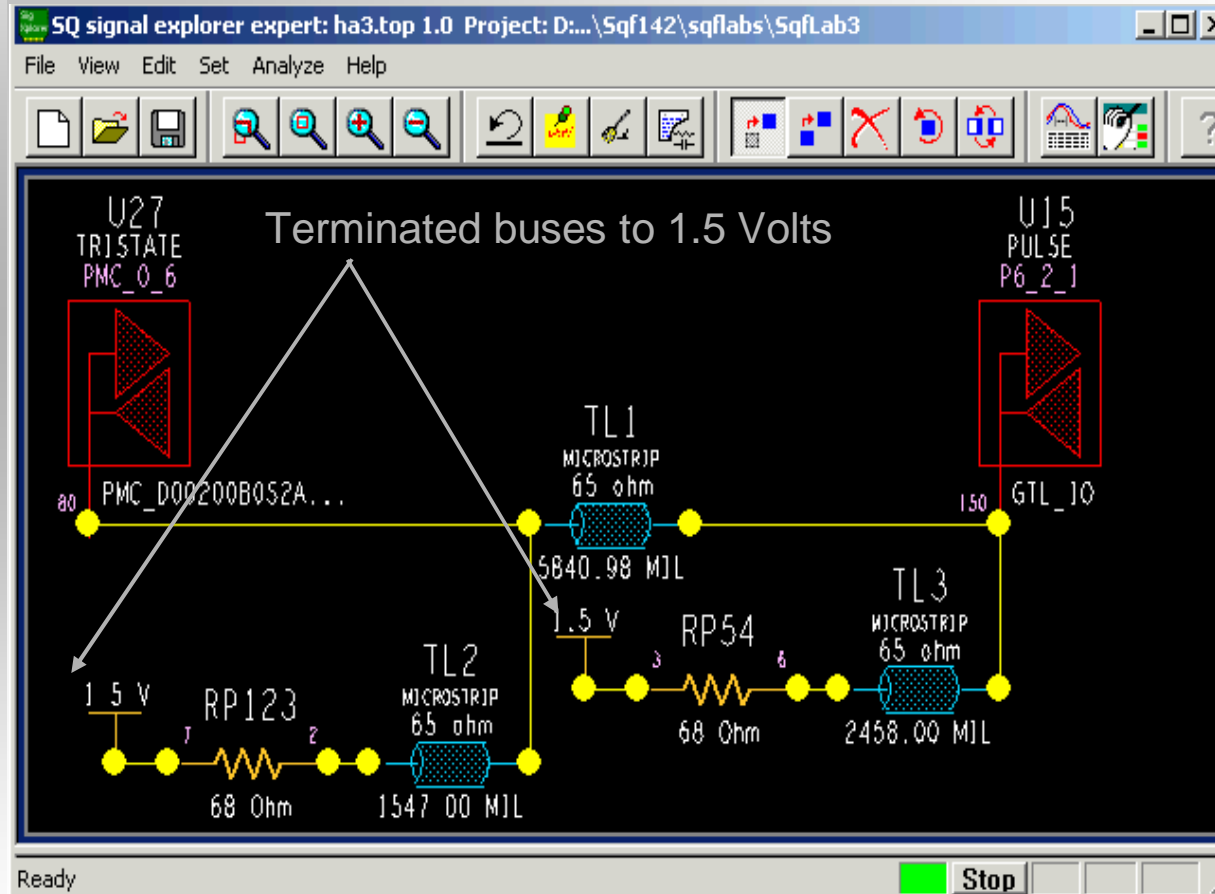
Loss Tangent: []

Differential Mode

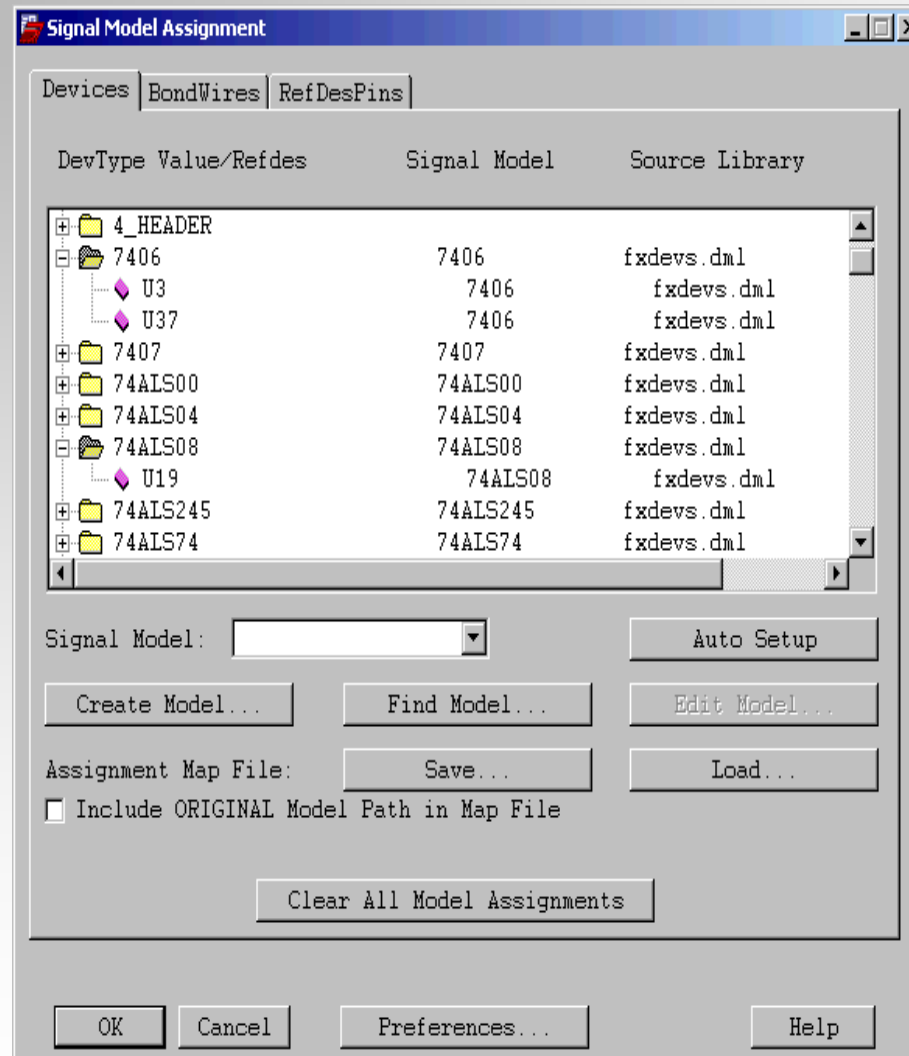
OK Apply Cancel Help

DC Voltages

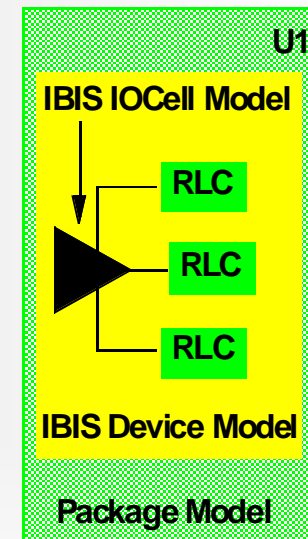
SPECCTRAQuest SI Expert needs source voltages for terminators and capacitors to build an electrically correct circuit.



Signal Model Assignment Form

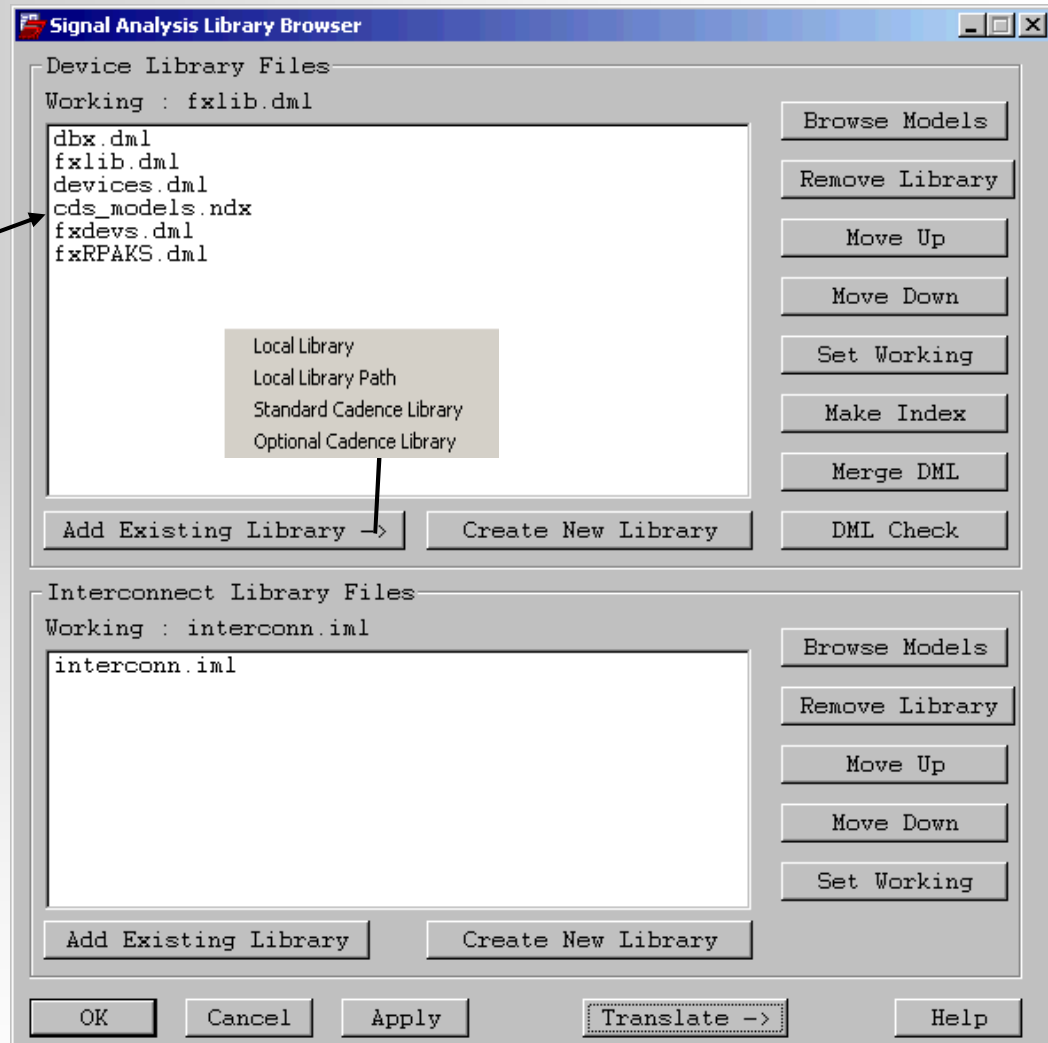


Signal Model



Translating and Adding Libraries

An Index file (.ndx) is a group of library files that have been merged and indexed together. You can use the models for simulation, but cannot modify the index file in any way.



You can translate these types of signal models to SPECCTRAQuest format.



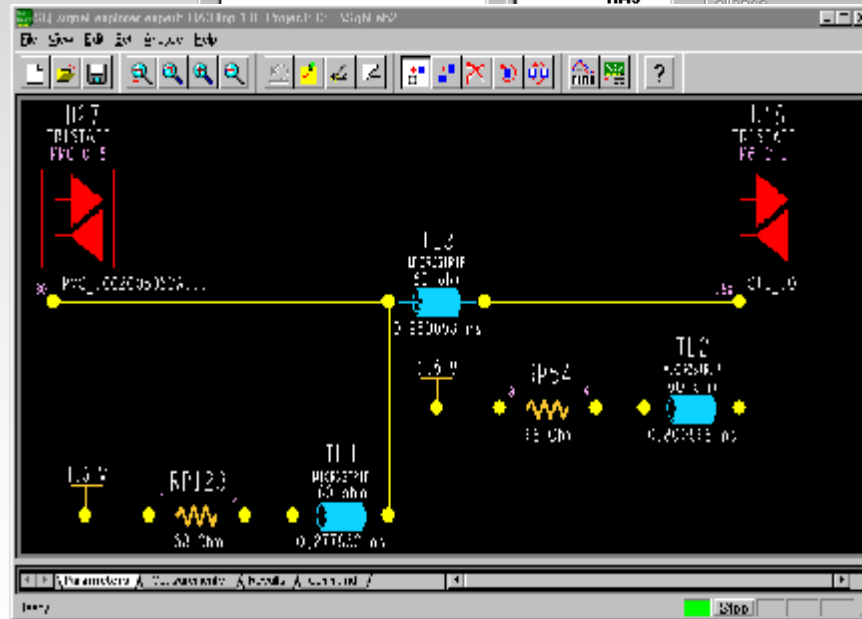
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Pre-Route Template Extraction

The Xnet includes the drivers, receivers and interconnects of an extended net.

The screenshot shows the 'Constraint Manager' window with the following table of objects and propagation delay data:

| Objects | Reference Electrical CSet | Pin Pairs | Prop Delay | | | Prop Delay | | |
|-------------------|---------------------------|-----------|------------|--------|--------|------------|--------|--------|
| | | | Min ns | Actual | Margin | Max ns | Actual | Margin |
| @FX.FX(SCH_1):GNT | | | | | | | | |
| @FX.FX(SCH_1):HA | | | | | | | | |
| HA3 | | | | | | | | |
| HA4 | | | | | | | | |
| HA5 | | | | | | | | |
| HA6 | | | | | | | | |
| HA7 | | | | | | | | |
| HA8 | | | | | | | | |
| HA9 | | | | | | | | |



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SQ Signal Explorer Expert Parameters Tab

The screenshot displays the SQ Signal Explorer Expert Parameters Tab. The top part shows a circuit diagram with components U27 (1R1STATE P4C_0_6), U15 (PULSE P6_2_1), TL1 (65 ohm), TL2 (63 ohm), TL3 (65 ohm), RP123 (63 Ohm), and RP54 (63 Ohm). The bottom part shows a table of parameters for the selected component (TL1).

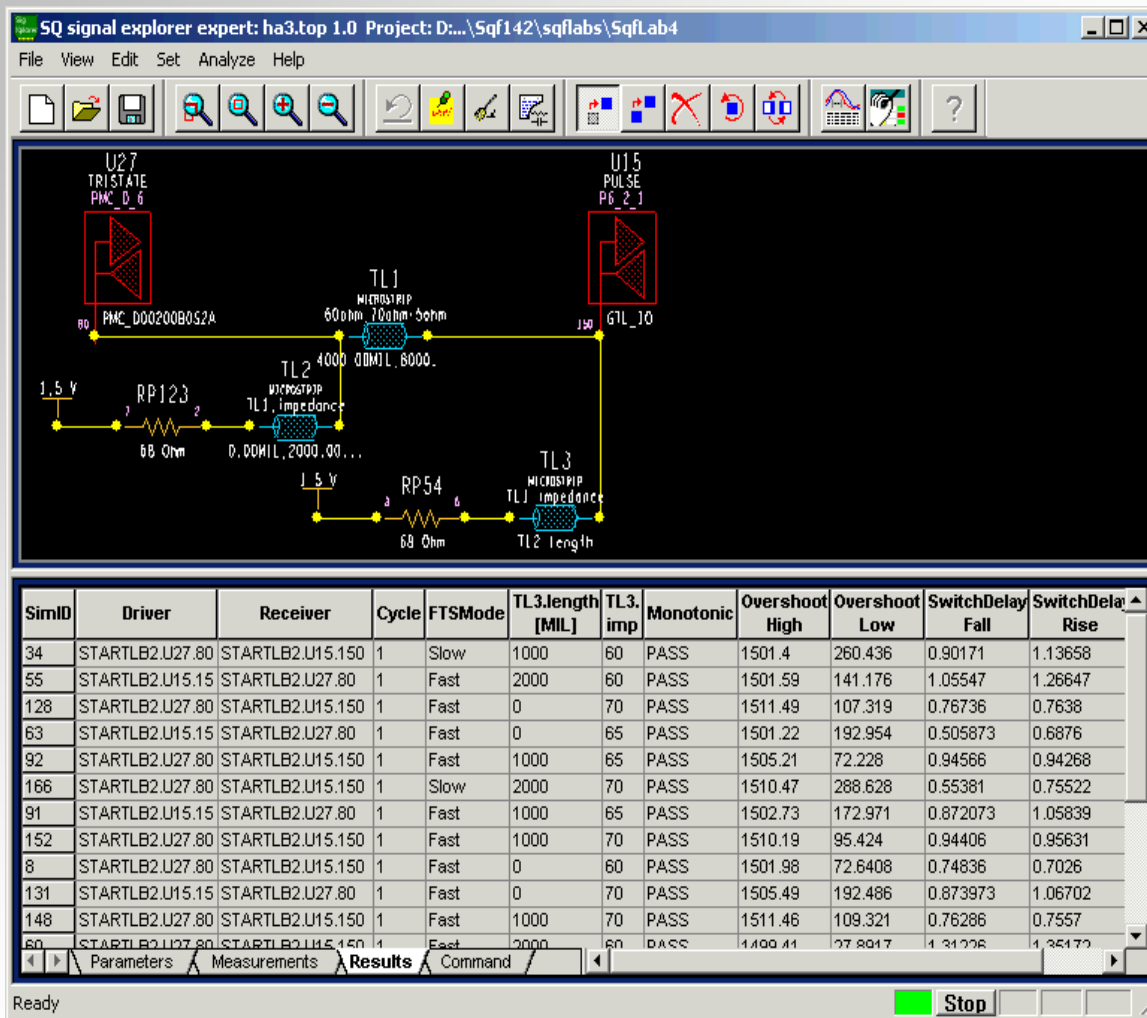
| Name | Value | Count |
|---|----------------|-------|
| <input type="checkbox"/> CIRCUIT | | 1 |
| tlineDelayMode | length | |
| userRevision | 1.0 | |
| <input type="checkbox"/> STARTLB2 | | |
| <input checked="" type="checkbox"/> RP54 | | |
| <input checked="" type="checkbox"/> RP123 | | 1 |
| <input type="checkbox"/> TL1 | | 1 |
| impedance | 65 ohm | 1 |
| length | 5840.98 MIL | 1 |
| traceGeometry | Microstrip | 1 |
| velocity | 5567.72 mil/ns | 1 |
| <input checked="" type="checkbox"/> TL2 | | 1 |

Toggle to display the units on the TLine to Length or Time.

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SQ Signal Explorer Expert Results Tab

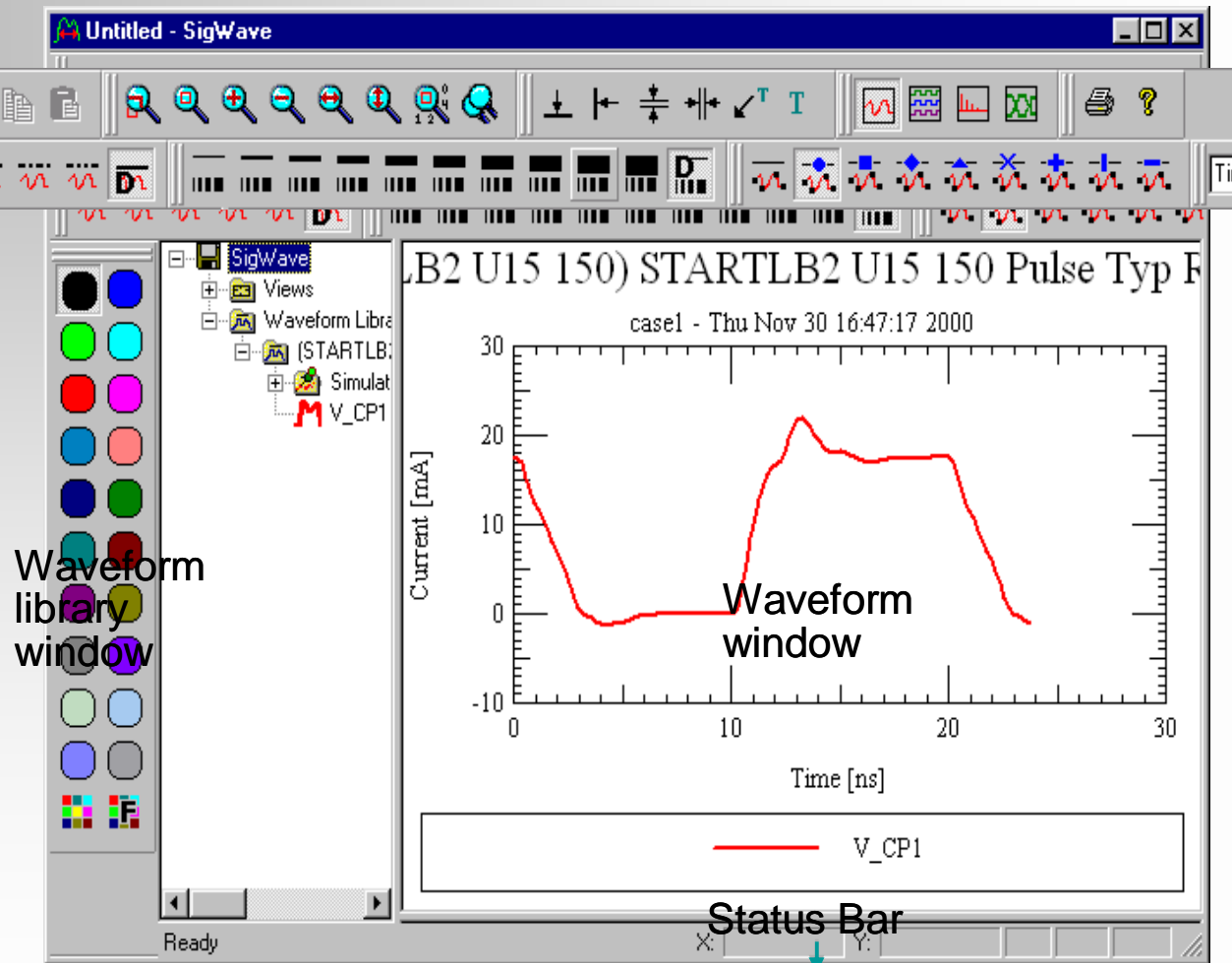


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SigWave Current Waveforms

Menu Bar

Tool Bar

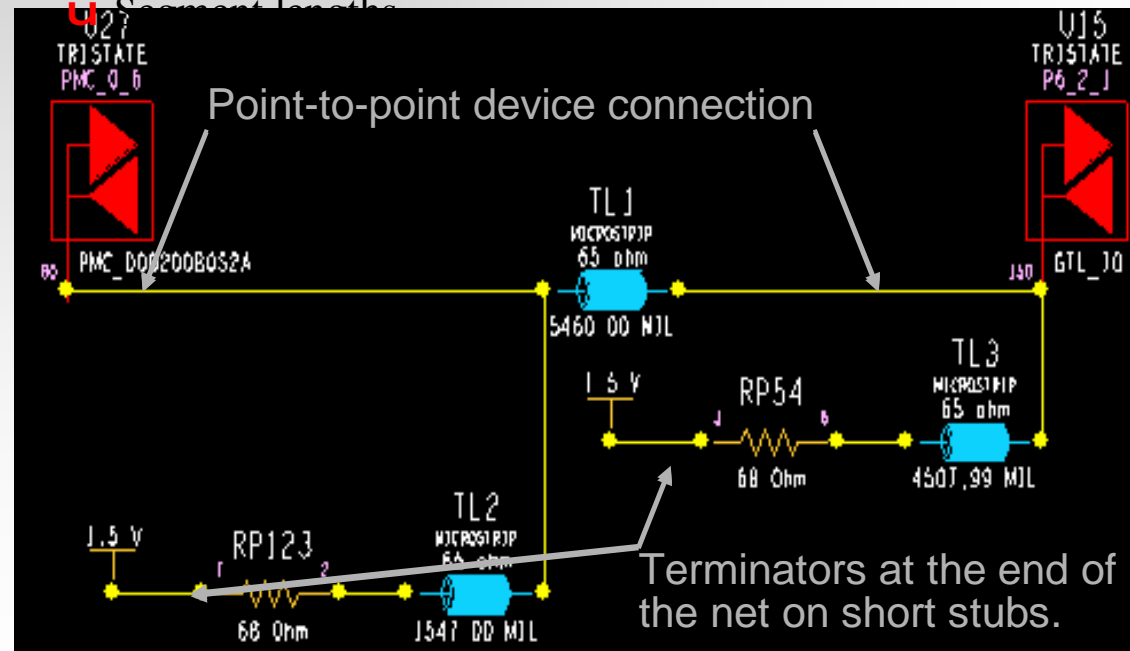


Waveform library window

Status Bar

Solution Space Analysis Step 1

- ∅ Extract / create topology to be analyzed.
 - ü Pin ordering
 - ü Discrete devices
 - ü Rat-T positions (if any)
- ∅ Identify / enter nominal values for all parameters.
 - ü Board impedance
 - ü Trace velocity
 - ü Terminator value
 - ü Segment lengths



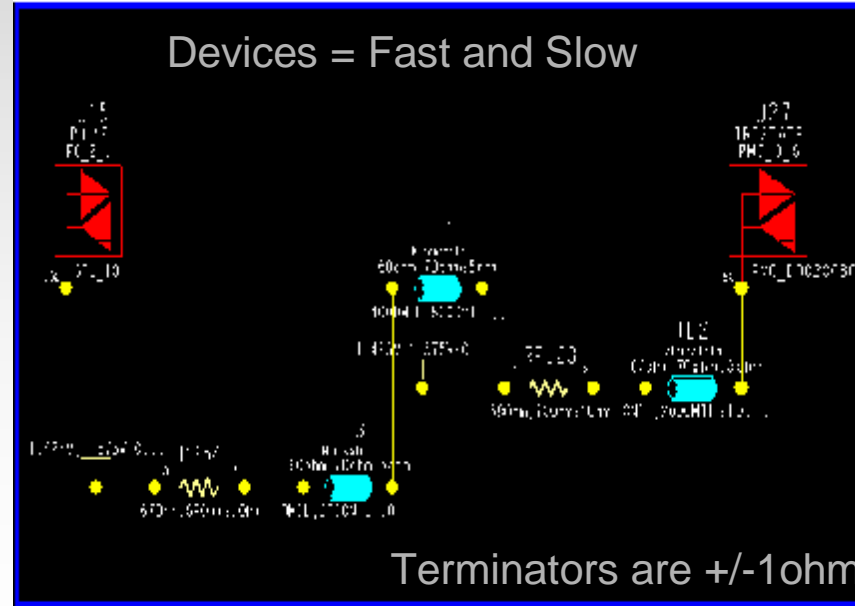
Solution Space Analysis Step 2

- ∅ Identify manufacturing variances that are to be included in the analysis.
 - ü Trace impedance (for example +/- 10%)
 - ü Trace velocity
 - ü Fast / slow components
 - ü Device values (ex. terminators)
 - ü Power supplies (if applicable)

- ∅ Identify initial ranges for “design rule” parameters.

- ü Min / max segment lengths

1.5 volt supply is +/- 5%



Trace impedance is 65 ohms +/- 5 ohms.

Trace length varies for each TLine:
TL1: 4000 mils to 8000 mils,
TL2 and TL3: 0 mils to 2000 mils.

Solution Space Analysis Step 3

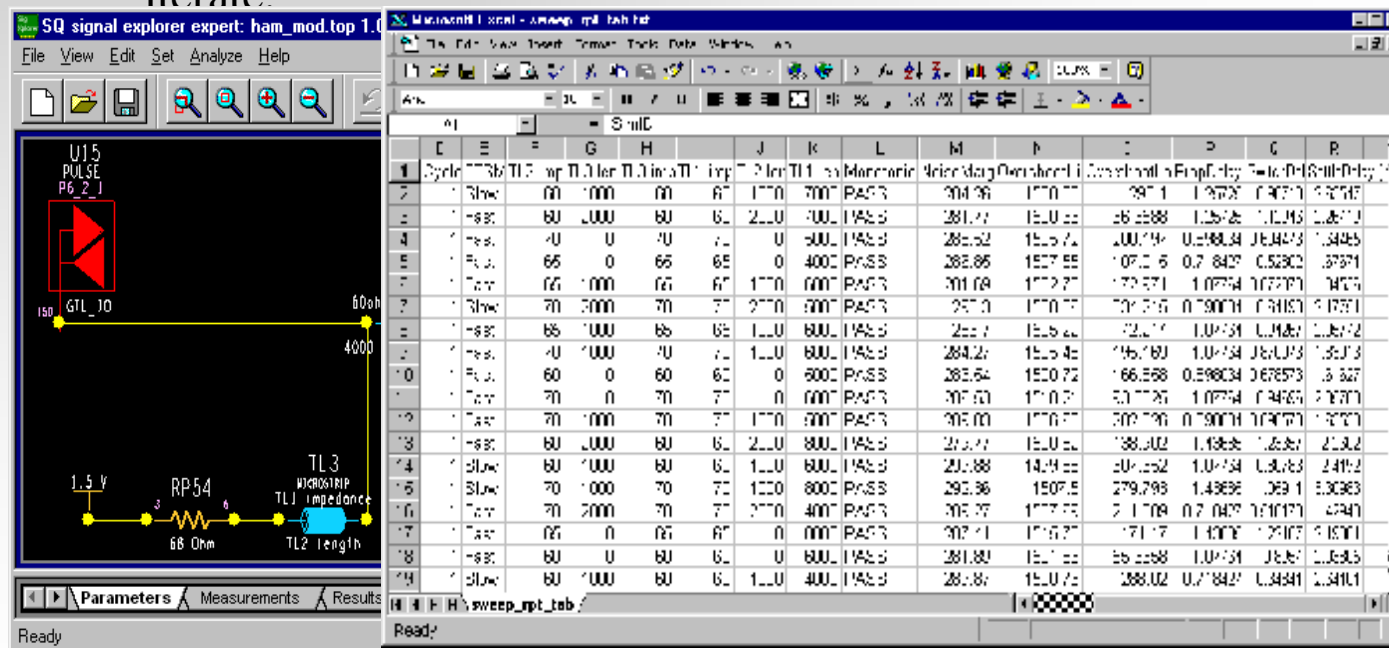
- ∅ Create a “master list” of all variables for analyses and their ranges.
- ∅ Identify “dependencies” between variables, based on how the design will be implemented.
 - ü Traces on the same layer have identical characteristics.
 - ü Resistors in the same RPAK match closely.

∅ Design parameters and dependencies to be

| Parameter | Min | Typ | Max | # Steps |
|---------------------------|--------------|---------------|--------------|------------|
| P6 Speed | Fast | | Slow | 2 |
| 440FX Speed | Fast | | Slow | 2 |
| TL1 Impedance | 60 ohms | | 70 ohms | 2 |
| TL1 Velocity | 5400 mils/ns | | 6600 mils/ns | 2 |
| TL1 Length | 4000 mils | | 8000 mils | 2 |
| TL2 Impedance | | TL1 Impedance | | 1 |
| TL2 Velocity | | TL1 Velocity | | 1 |
| TL2 Length | 0 mils | | 2000 mils | 2 |
| TL3 Impedance | | TL1 Impedance | | 1 |
| TL3 Velocity | | TL1 Velocity | | 1 |
| TL3 Length | 0 mils | | 2000 mils | 2 |
| RP A Impedance | 67 ohms | | 69 ohms | 2 |
| RP B Impedance | 67 ohms | | 69 ohms | 2 |
| Total Combinations | | | | 512 |

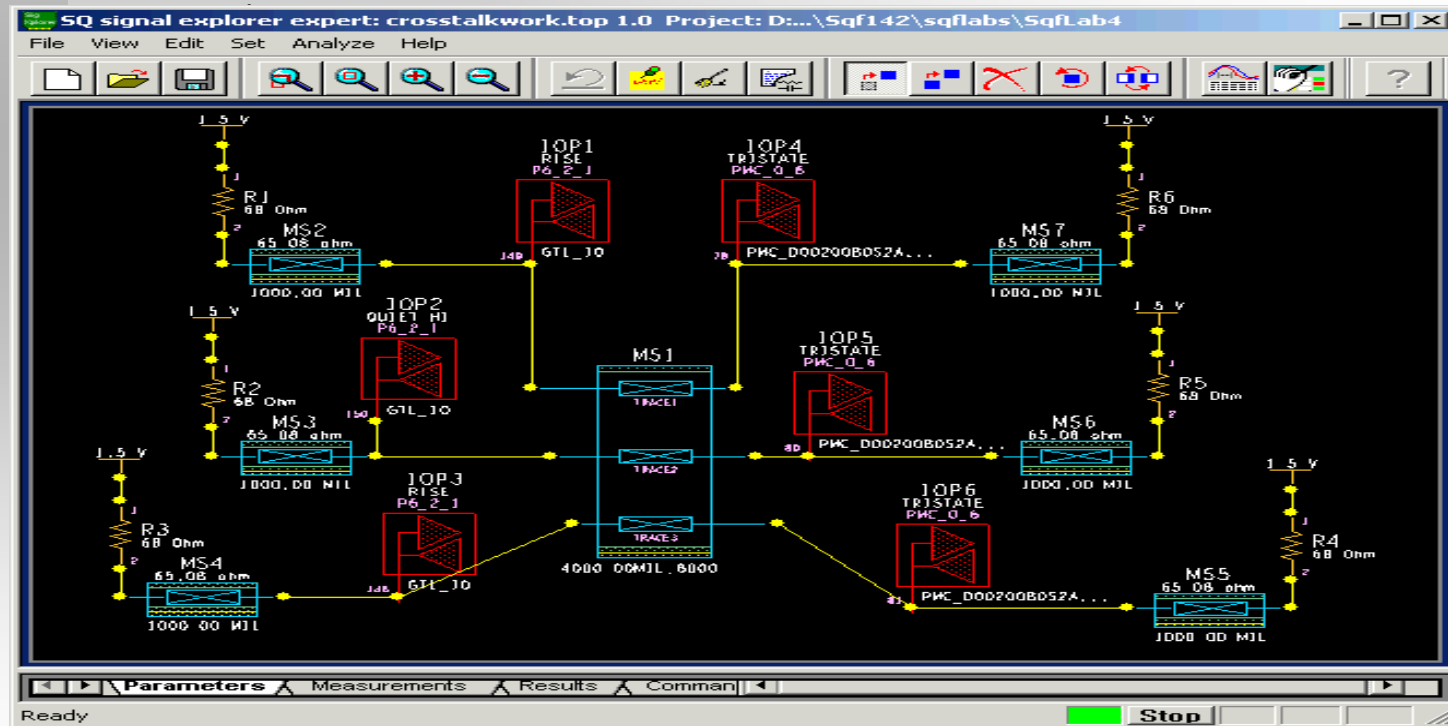
Solution Space Analysis Step 4

- Ø Run simulations and gather results.
 - ü SigXp “tabbed” report format is designed to import easily into Microsoft Excel and Access.
- Ø Evaluate results and identify “cases” (combinations of variables) that cause topology to fail (not meet design goals).
- Ø Simulate individual cases, analyze, correct design if needed, and iterate.



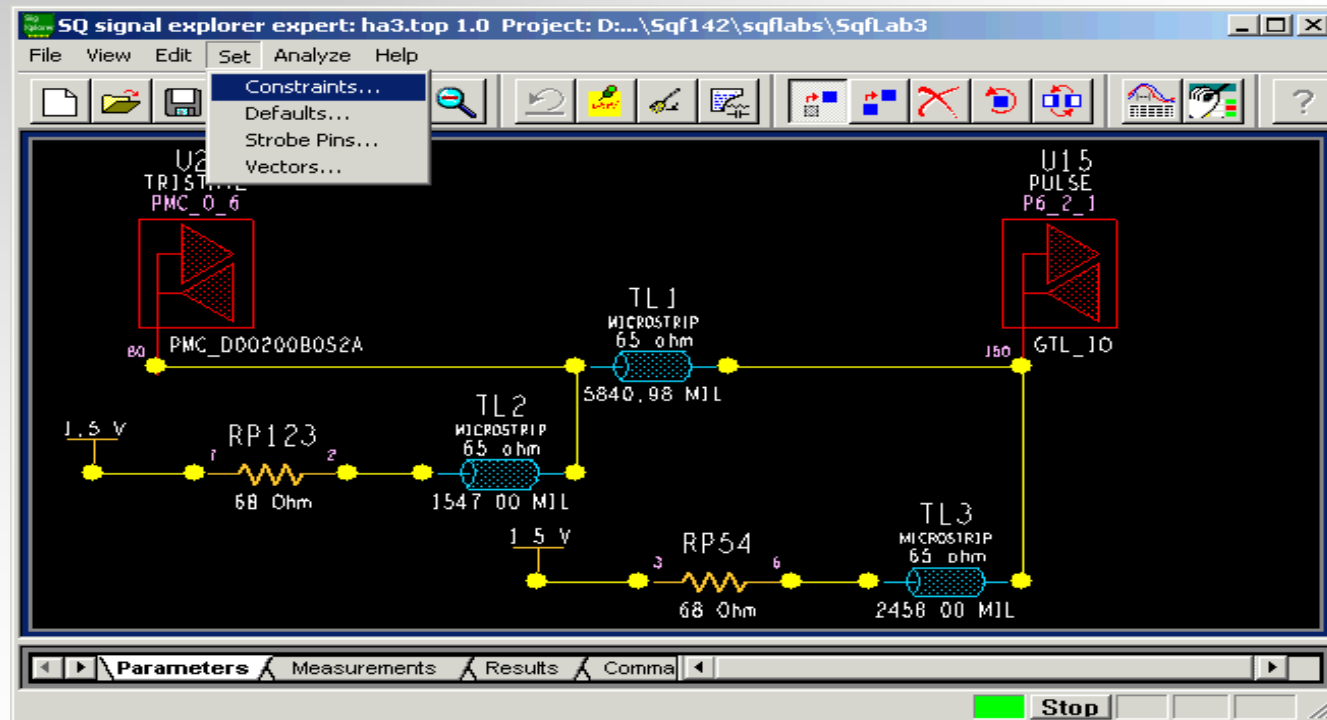
Solution Space Analysis Step 5

- ∅ The solution found thus far is a single-line solution.
- ∅ Crosstalk timing shifts must be within crosstalk budget.
- ∅ Single-line topology is modified to model coupling where appropriate.
- ∅ Different line width / spacing rules are evaluated for timing



Solution Space Analysis Step 6

- ∅ Create final topology template from analysis results:
 - ü Segment min / max lengths
 - ü Parallelism rules
- ∅ Some variances should not be included in the final topology template:



Terminators are +/-1ohm

Parametric Sweeps

SQ signal explorer expert: ham_mod.top 1.0 Project: C:\...\SqLab3

File View Edit Set Analyze Help

TL1
MICROSTRIP
60ohm, 70ohm, 5ohm
4000.00MIL, 8000.00MIL

| Name | Value | Count |
|---------------|---------------------------------------|-------|
| TL1 | | 3 |
| impedance | 60 ohm, 70 ohm: 5 ohm | 3 |
| length | 4000.00 MIL, 8000.00 MIL: 1000.00 MIL | 5 |
| traceGeometry | Microstrip | 1 |
| velocity | 5567.72 mil/ns | 1 |
| TL2 | | 3 |

Parameters Measurements Results Command

Ready

Set Parameter: length

Single Value
 Single Value Value

Linear Range
 Linear Range
 Start Value: 4000.00 MIL
 Stop Value: 8000.00 MIL
 Count: 5
 Step Size: 1000.00 MIL

Multiple Values
 Multiple Values
 Insert Value
 Delete Value
 TextEdit...

Expression
 Expression

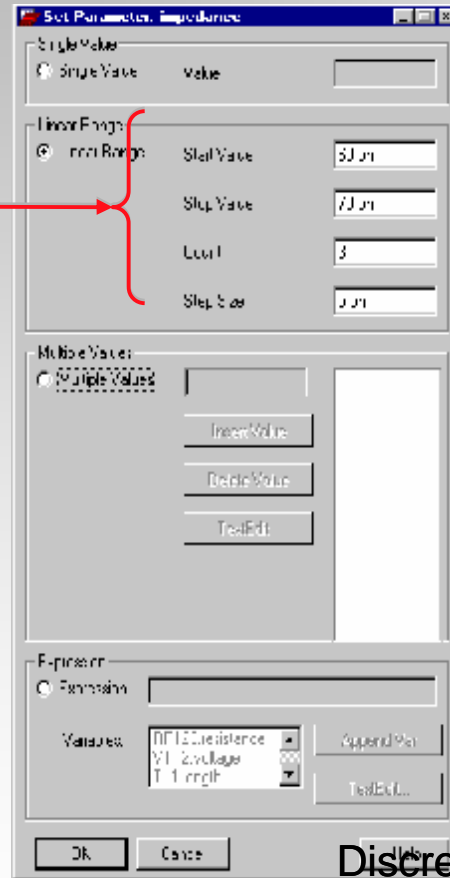
Variables: TL2.impedance, TL2.length
 Append Var
 TextEdit...

OK Cancel Help

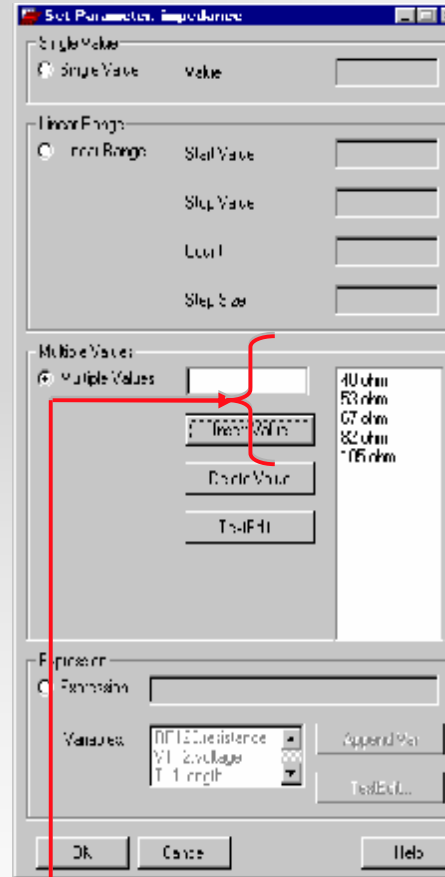
Sweep parameters are chosen by setting a start and stop value. The count value determines the number of sweep count points.

Setting Sweep Parameters

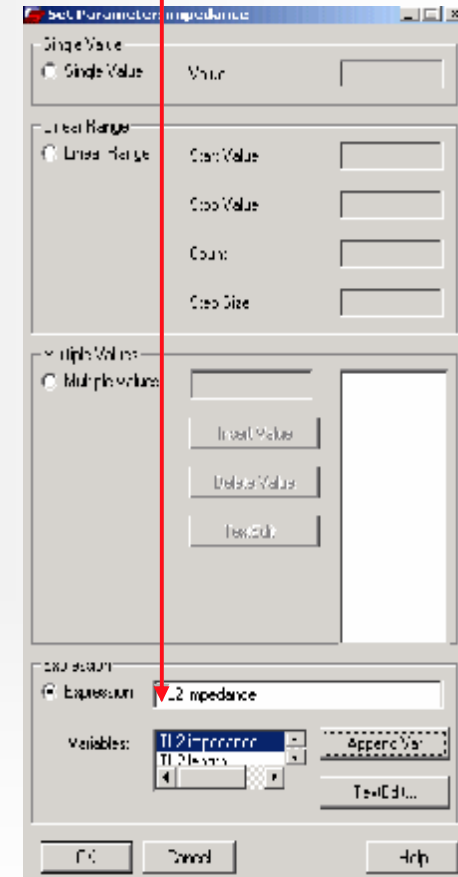
Count value determines the number of sweep count points.



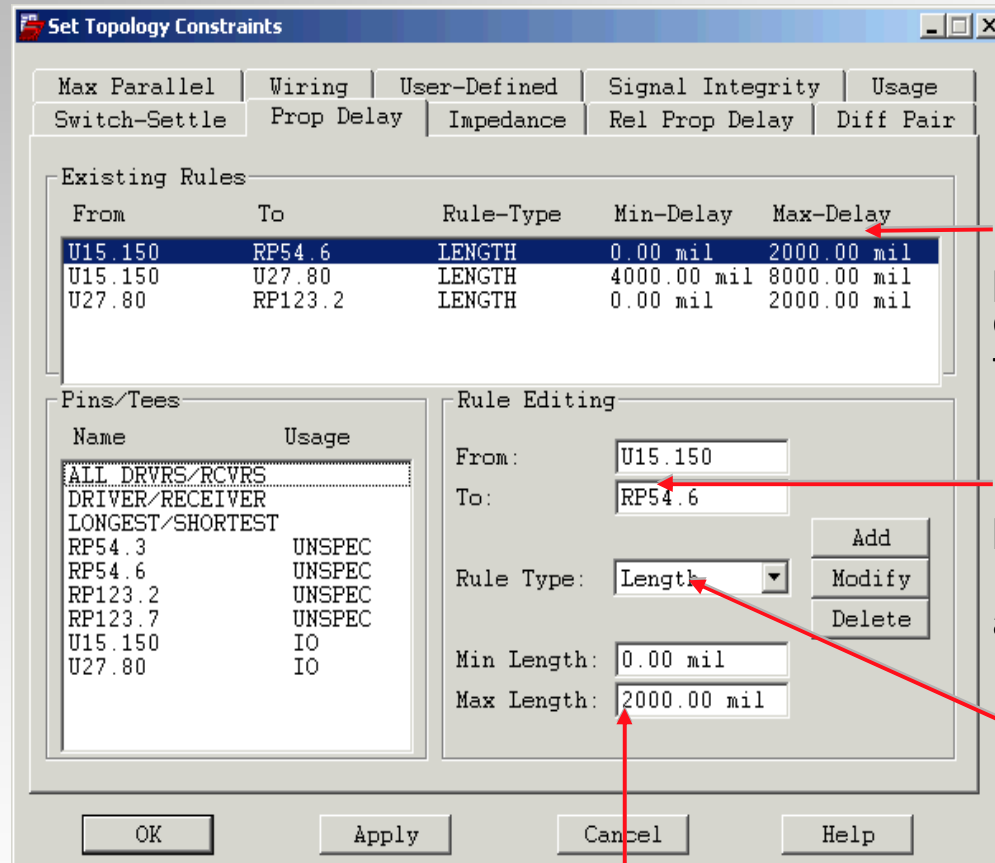
Expression listed and other parameters used in the expression determine the number of sweep count points.



Discrete values determines the number of sweep count points.



Assigning Prop Delay Constraints



List the Pin or Pin-Tee pairs that have delay constraints assigned in the current topology.

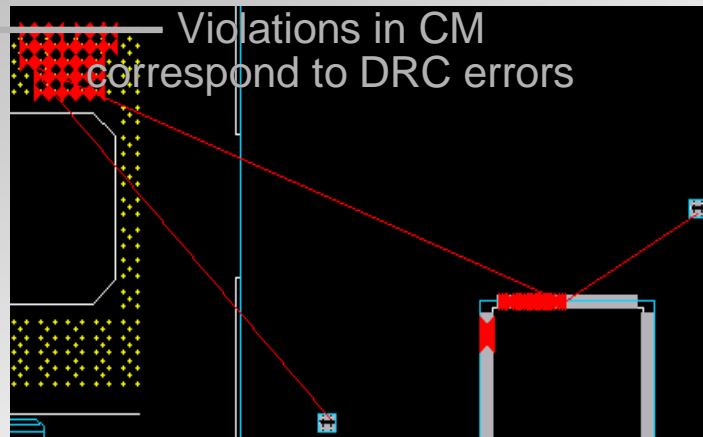
Identify the desired points between which Prop Delay constraint is to be applied.

Delay Length % Manhattan

Components are listed with their pinuse values.

Identify the desired min and max delay acceptable for this pair.

Template Applications and Constraint-Driven Placement



Constraint values

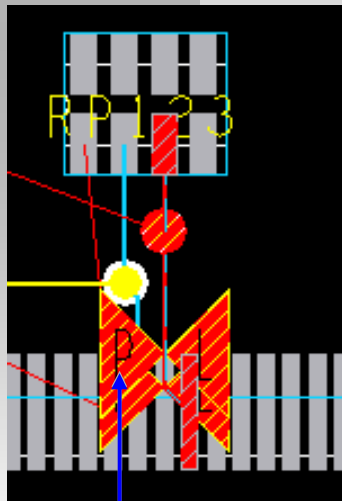
Actual manhattan routing distance

Worst case bubbles to the top

| Referenced Electrical CSet | Pin Pairs | Prop Delay | | | Prop Delay | | |
|----------------------------|-----------|------------|-----------|-----------|------------|------------|------------|
| | | Min | Actual | Margin | Max | Actual | Margin |
| | | ns | | | ns | | |
| HA3 | | | | | | -17607 MIL | |
| HA3 | | | | | | -2508 MIL | |
| | 0 MIL | 4508 MIL | 4508 MIL | 2000 MIL | 4508 MIL | -2508 MIL | |
| | 4000 MIL | | | 8000 MIL | 5460 MIL | 2540 MIL | |
| | 0 MIL | | | 2000 MIL | 1547 MIL | 453 MIL | |
| HA4 | HA3 | | | | | -17607 MIL | |
| U15.149:RP48.4 | | 0 MIL | 19607 MIL | 19607 MIL | 2000 MIL | 19607 MIL | -17607 MIL |
| U15.149:U27.78 | | 4000 MIL | | | 8000 MIL | 5600 MIL | 2400 MIL |
| U27.78:RP123.3 | | 0 MIL | | | 2000 MIL | 1538 MIL | 462 MIL |
| HA5 | HA3 | | | | | -8557 MIL | |
| U15.140:RP124.3 | | 0 MIL | 10557 MIL | 10557 MIL | 2000 MIL | 10557 MIL | -8557 MIL |
| U15.140:U27.83 | | 4000 MIL | | | 8000 MIL | 5301 MIL | 2699 MIL |
| U27.83:RP60.6 | | 0 MIL | 8735 MIL | 8735 MIL | 2000 MIL | 8735 MIL | -6735 MIL |
| HA6 | HA3 | | | | | -10422 MIL | |
| U15.148:RP55.1 | | 0 MIL | 12422 MIL | 12422 MIL | 2000 MIL | 12422 MIL | -10422 MIL |
| U15.148:U27.77 | | 4000 MIL | | | 8000 MIL | 5720 MIL | 2280 MIL |
| U27.77:RP123.4 | | 0 MIL | | | 2000 MIL | 1549 MIL | 451 MIL |

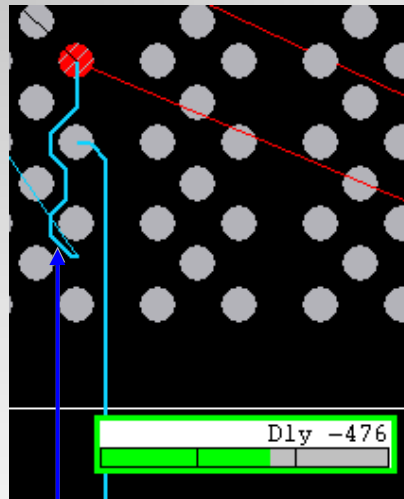
Constraint-Driven Routing

Bubble: Off



The spacing rule violation flagged off by DRC markers

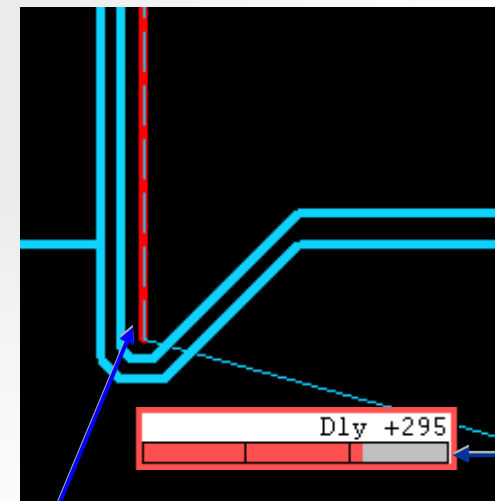
Bubble: Hug Preferred



The etch that is routed hugs the object to avoid DRC violation.

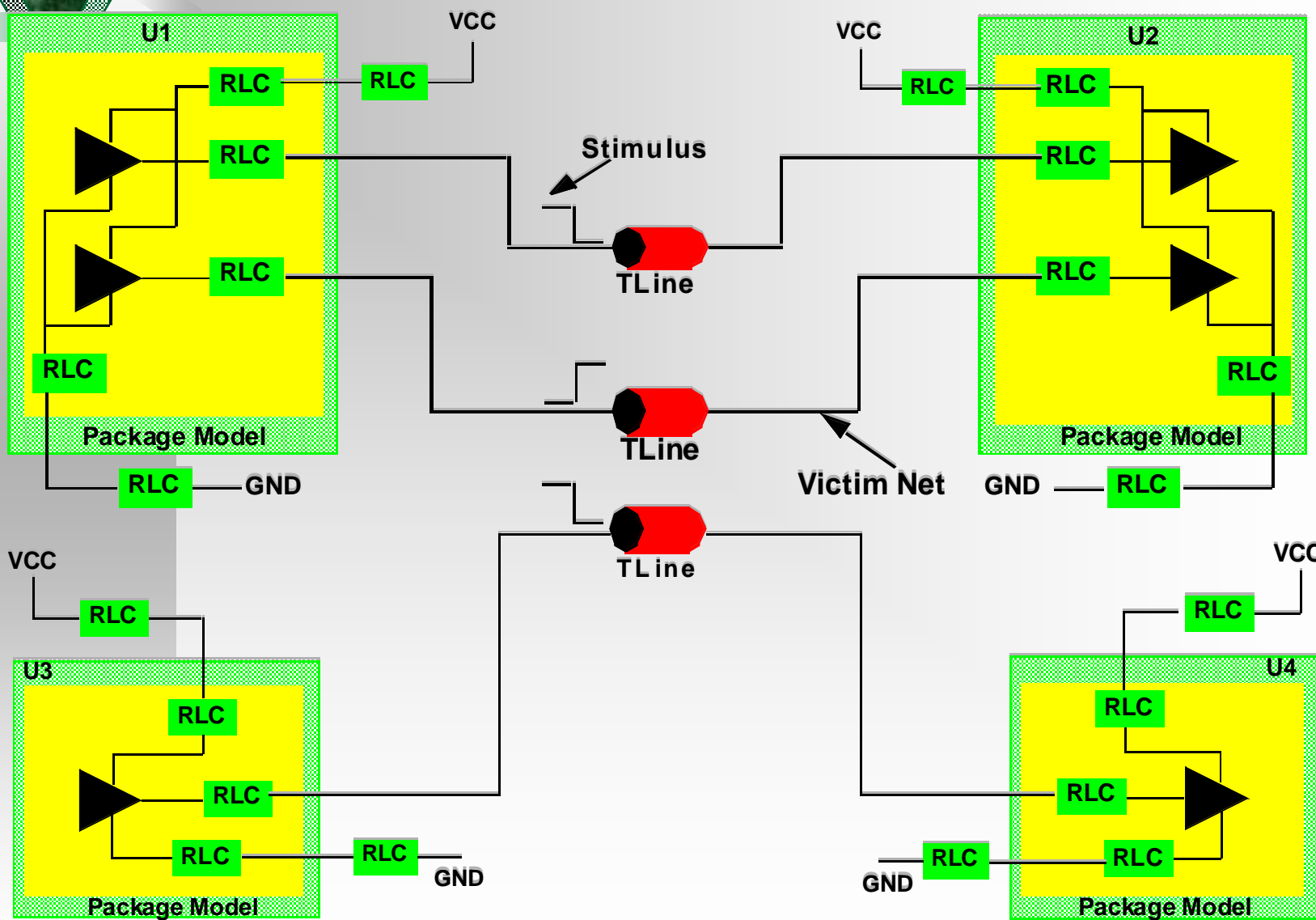
Dynamic timing meter highlights high-speed timing constraint violation.

Bubble: Shove Preferred

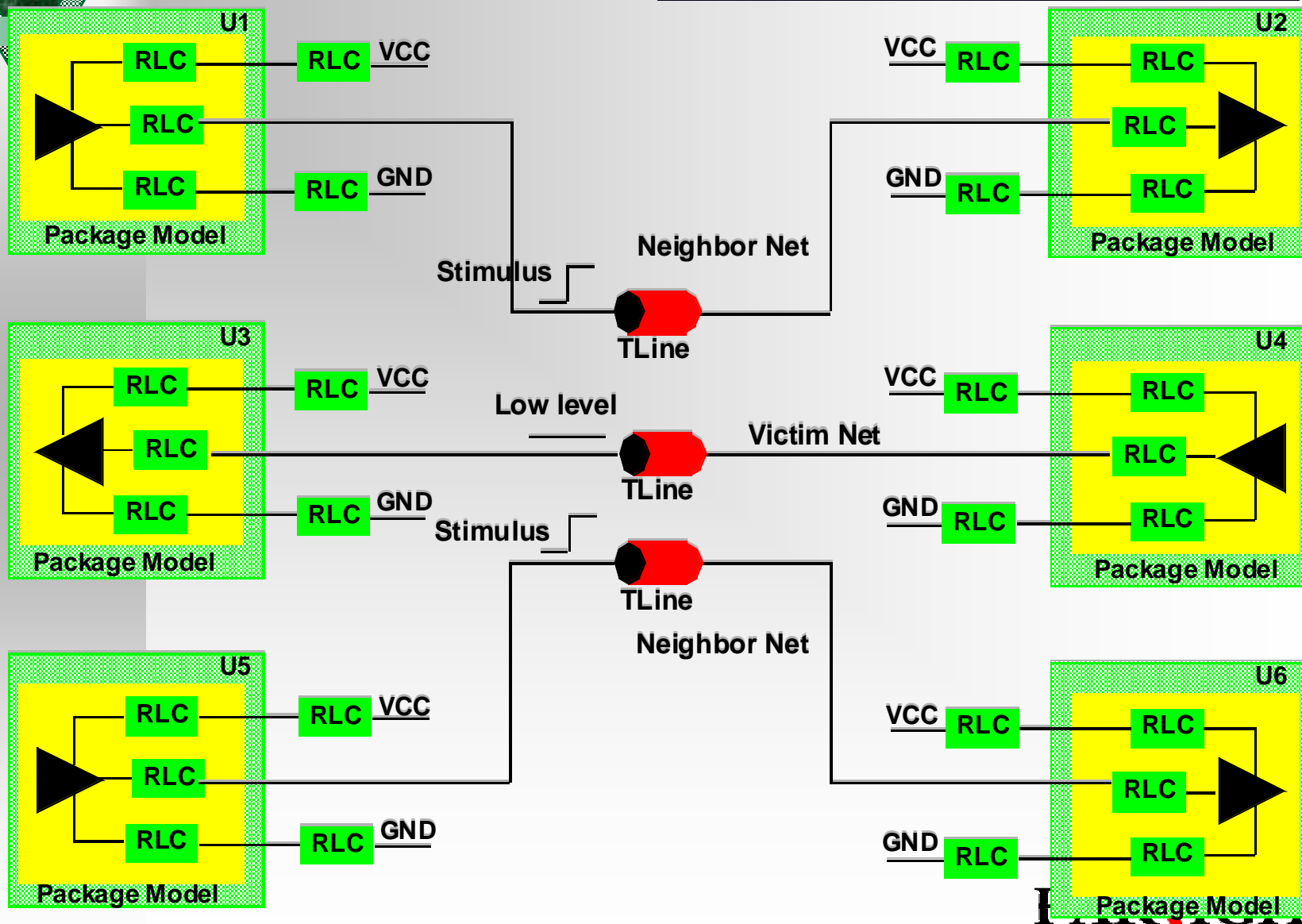


The etch that is routed pushes the existing etch to resolve DRC violation.

Post-Route DRC and Analysis



Crosstalk Simulation



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Simultaneous Switching Noise Report

Results from a SSN simulation:

```
*****
Simultaneous Switching Noise (mV) for XNet `2 COMPLETE HA4` (Typ FTSMODE)
*****
Drvr          Net          PowerBus  SSNRise  GroundBus  SSNFall
-----
COMPLETE U15 149  COMPLETE HA4  pwrctl   0          gndbus    51.54
-----

*****
Driver I/O Characteristics (Typ FTSMODE) RiseSlew/FallSlew in (mV/ns)
*****
Drvr          IOModel  Volmax  Vohmin  RiseSlew  FallSlew
-----
COMPLETE U15 149  GTL_IO  400 mV  3000 mV  271       284
-----

*****
Load I/O Characteristics
*****
Rcvr          IOModel          Vilmax  Vihmin
-----
COMPLETE U27 78  PMC_D00200B0S2AZZGHE  800 mV  1200 mV
-----

*****
Pulse Data Per Xnet
*****
XNet          PulseFreq  PulseDutyCycle  PulseCycleCount
-----
2 COMPLETE HA4  66MHz      0.5              1
-----

*****
```

System-Level Analysis

The screenshot shows the 'System Configuration Editor' window. It is divided into several sections:

- Drawings:** Contains buttons for 'Add File', 'Add BoardModel', 'Remove', 'Set Design Name', and 'Set Drawing Path'. Below these is a list of drawings: 'A complete.brd' and 'B daughter.brd'. A red oval annotation points to this list with the text 'Two layouts identified for this DesignLink'.
- Connections:** Contains buttons for 'Add', 'Remove', 'Copy', 'Set Length', and 'Set Cable Model'. Below these is a list of connections: 'DIAPINS' and 'OMETER'. A red oval annotation points to this list with the text 'Connection, length and RLGC cable model identified'.
- System Xnets Names From Design:** A dropdown menu currently set to 'A'.
- Connection PinMap:** Contains buttons for 'Add Wires', 'Remove Wires', 'Connect by Component', and 'TextEdit PinMap'. Below these are 'Set From Pin(s)' and 'Set To Pin(s)' buttons.
- Wire(s) Table:** A table with three columns. The first column is highlighted with a yellow box and annotated with 'Number of wires in this connection'. The second column is highlighted with a cyan box and annotated with 'Connections on the first board'. The third column is highlighted with a magenta box and annotated with 'Connections on the second board'.

| Wire(s) | Set From Pin(s) | Set To Pin(s) |
|-----------|-----------------------|---------------------|
| 1 - 49 | A J12 A1 - A J12 A49 | B J1 A01 - B J1 A49 |
| 50 - 60 | A J12 A52 - A J12 A62 | B J1 A52 - B J1 A62 |
| 61 - 109 | A J12 B1 - A J12 B49 | B J1 B01 - B J1 B49 |
| 110 - 120 | A J12 B52 - A J12 B62 | B J1 B52 - B J1 B62 |

At the bottom of the window are 'OK', 'Cancel', and 'Help' buttons.

Differential Pair Design Exploration

Constraint Manager (connected to SPECCTRAQuest SI Expert 15.0) - [Nets: Routing]

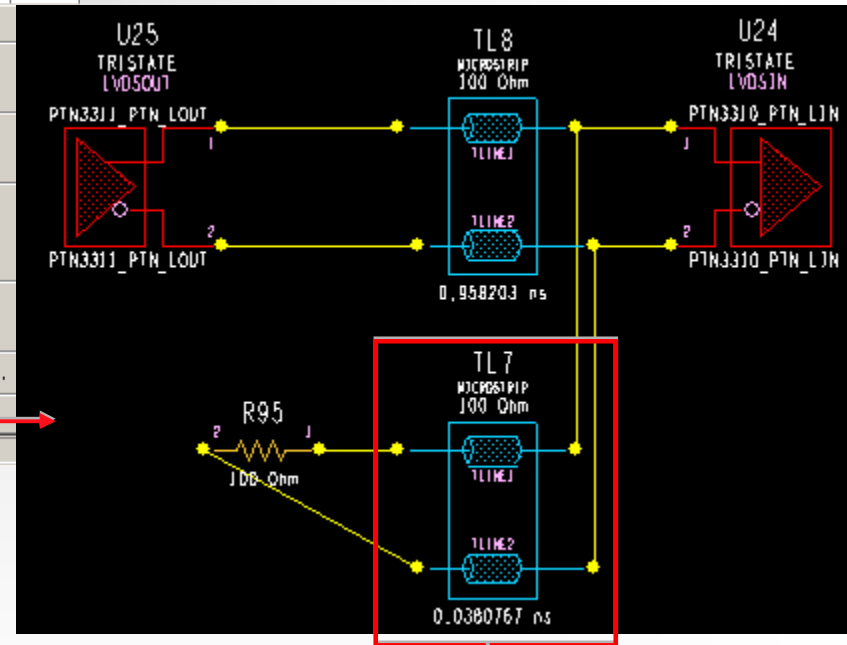
File Edit Objects Column View Analyze Audit Tools Window Help

Electrical Constraint Set

- Signal Integrity
- Timing
- Routing
- All Constraints
- Net
 - Signal Integrity
 - Timing
 - Routing
 - Wiring
 - Impedance
 - Min/Max Propagation Delay
 - Total Etch Length
 - Differential Pair
 - Relative Propagation Delay
 - Custom Measurement

| Objects | Referenced Electrical CSet | Gather Contro |
|--------------------|----------------------------|---------------|
| XD5 | | |
| XD6 | | |
| XD7 | | |
| @FX.FX(SCH_1):XTAL | | |
| PWRGD | | |
| DIFFNET1 | | |
| NET1_M | | |
| NET1_P | | |
| DIFFNET2 | | |
| NET2_M | | |
| NET2_P | | |
| DIFFNET3 | | |
| NET3_M | | |
| NET3_P | | |
| A20M | | |
| ACK | | |
| AEN | | |
| AENR | | |
| AERR | | |
| AFD | | |
| AFDR | | |
| Total Etch Length | | |

Diff Pair: DIFFNET1



Extracted Ideal TlineCoupled model

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Custom Stimulus to Analyze Differential Pair Topology

IO Cell (U25) Stimulus Edit

Stimulus State

- Pulse
- Quiet Hi
- Rise
- Quiet Lo
- Fall
- Tristate
- Custom

Terminal Info

Terminal Name: DATA

Stimulus Type: SYNC

Stimulus Name: NONE

Measurement Info

Cycle(s): 1

Terminal Offset: 0 ns

Stimulus Editing

| Frequency | Init | Switch At | Pattern | Tr(0-100%) | Tf(0-100%) |
|-----------|------|-----------|---------------------|------------|------------|
| 400 MHz | 0 | BOTH | 1001 0011 1100 1010 | 0.583 ns | 0.55 ns |

CLOCKI

DATA

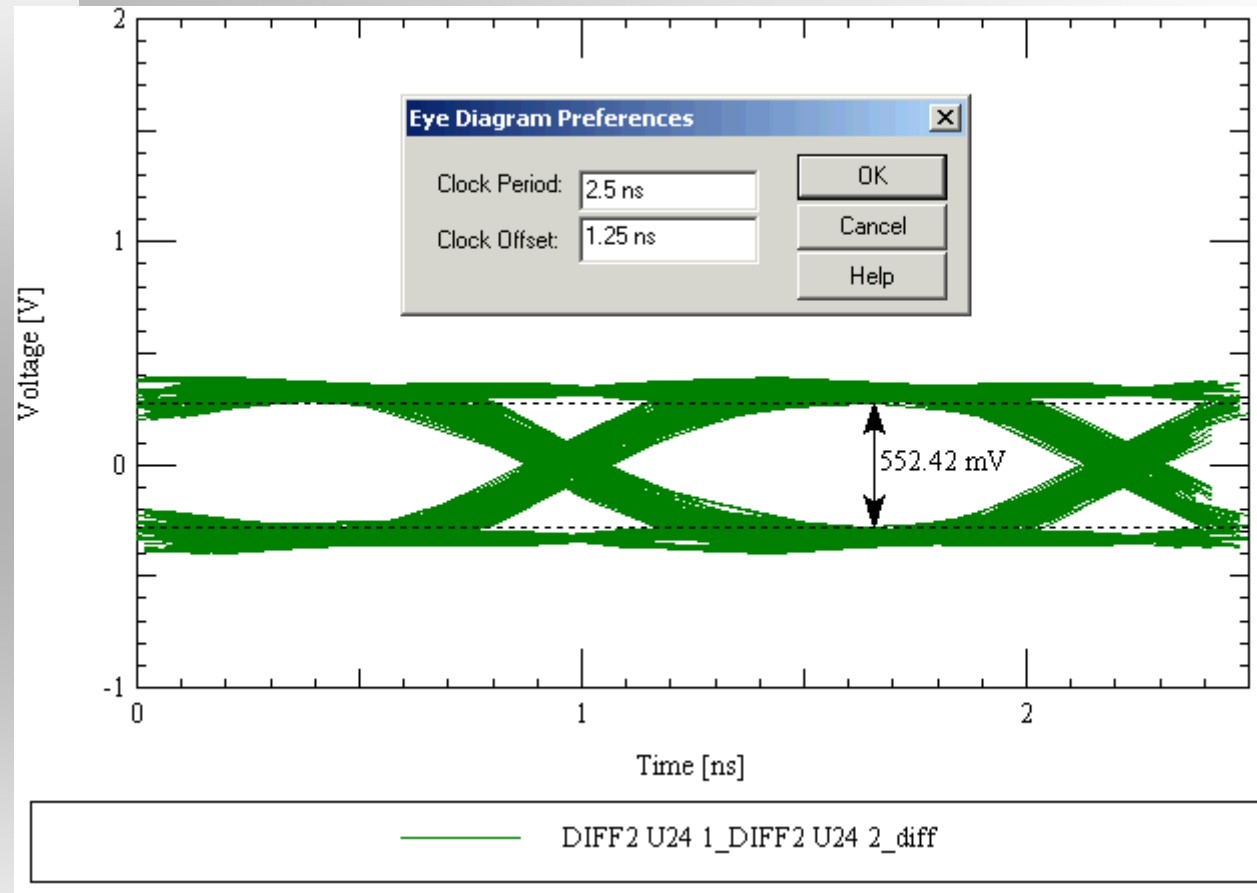
DATA_

0 ns 40 80 120 160 200

OK Apply Cancel Help

Maximum of 1024 bits

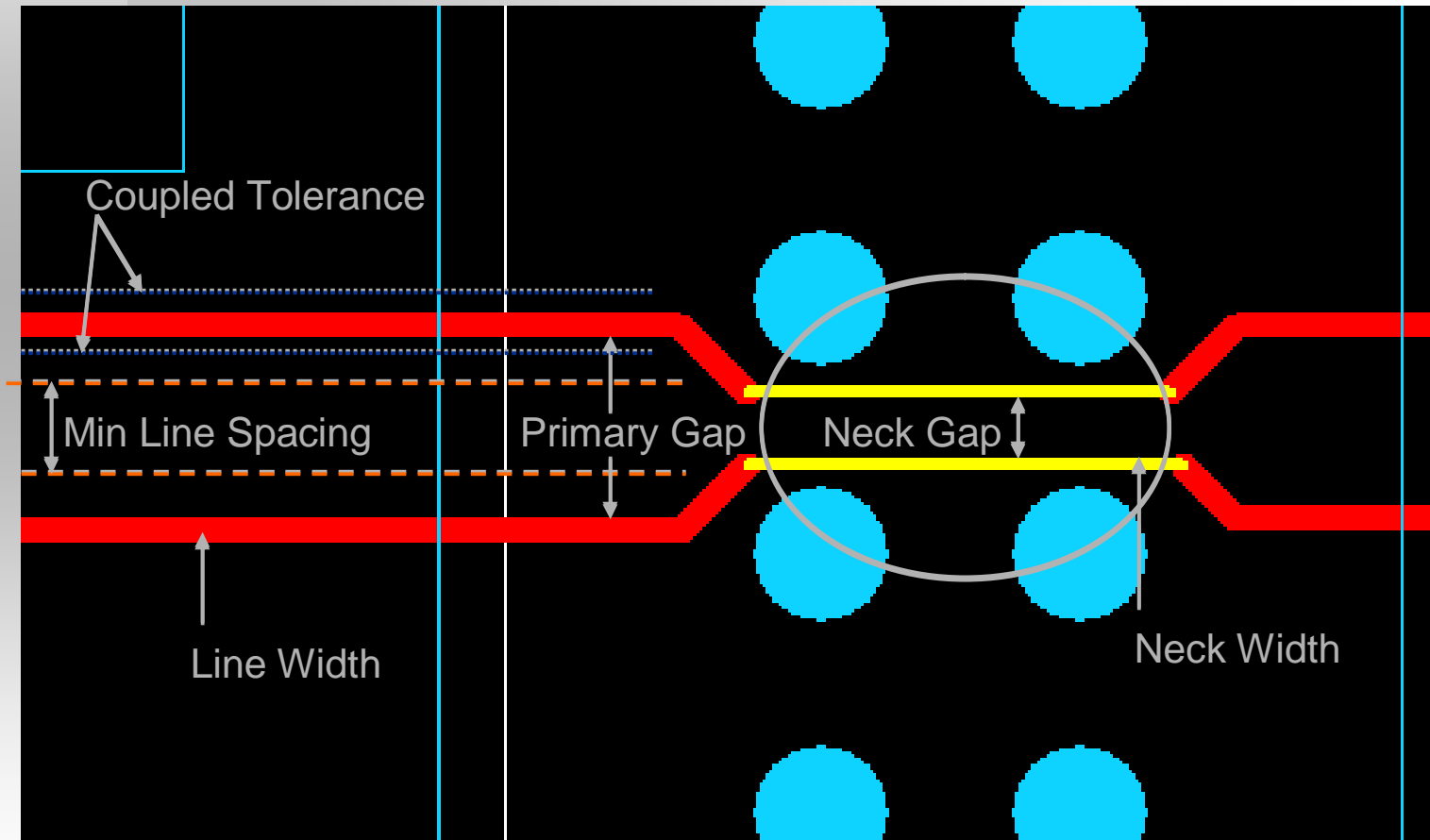
Differential Pair Topology Analysis



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Gap and Line Width

From the SPECCTRAQuest SI Expert menu, select **Route—Connect** command.



华清远见CADENCE相关课程

✓ 初级班(三天)

- ✓ 1. Concept HDL 原理图设计
- ✓ 2. Allegro PCB设计
- ✓ 3. Librarian Expert 库管理

✓ 高级班(三天)

- ✓ Day 1: Basic theories in high-speed PCB design
- ✓ Pre-Placement
- ✓ Extracting and Simulating Topologies
- ✓ Day 2: Determining and Adding Constraints
- ✓ Template Applications and Constraint-Driven Placement
- ✓ Day 3: Constraint-Driven Routing
- ✓ Post-Route DRC and Analysis
- ✓ Differential Pair Design Exploration

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让我们一起讨论！



FAR SIGHT



The success's road

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谢谢！