

The logo features the word "FAR SIGHT" in white, bold, sans-serif capital letters. A red, stylized vertical bar separates the "FAR" and "SIGHT" parts. The text is centered within a dark green, downward-pointing triangle that has a subtle, textured pattern. The triangle is set against a light gray background that forms a larger, faint downward-pointing triangle.

FAR SIGHT

嵌入式培训专家

高速电路设计与仿真
---SPECCTRAQuest Foundations

www.farsight.com.cn

问题的提出及课程目的

- ✓ 高速PCB设计失败的例子
- ✓ 系统地认识高速PCB设计中会遇到哪些棘手问题？这些问题有什么现象和表现形式？
- ✓ 理解问题产生的原因、机理
- ✓ 掌握问题的解决方法



华清远见

高速PCB设计中的主要问题

√ 信号完整性问题

√ 时序问题

√ 电磁兼容性问题

FAR SIGHT

高速PCB设计中的理论基础

✓ 传输线理论（高速PCB中所涉及的）

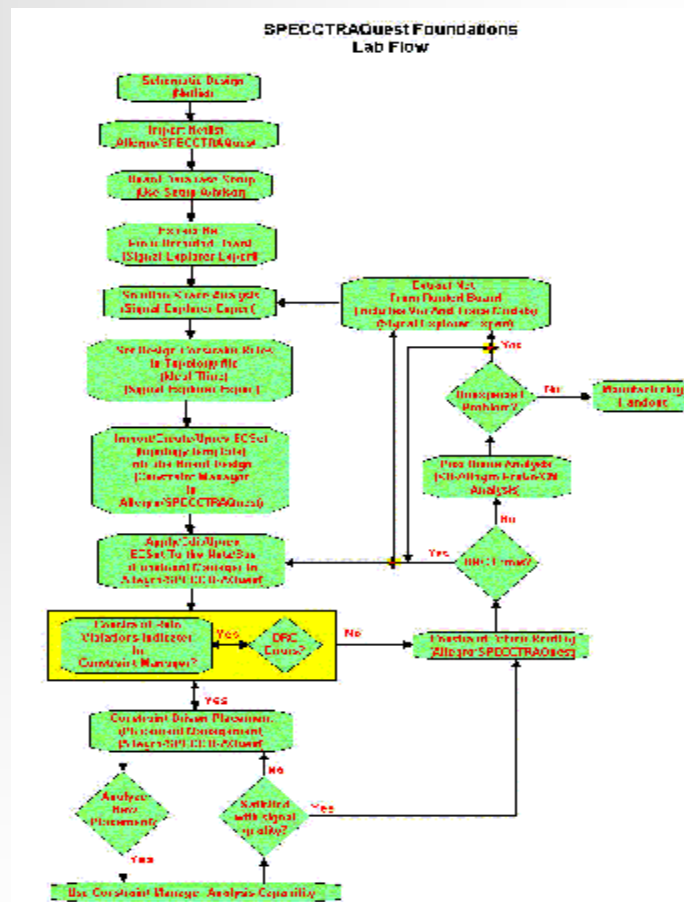
✓ 反射、串扰、振铃、地弹等

✓ 时序匹配

The SPECCTRAQuest Design Flow

The SPECCTRAQuest Design Flow consists of the following six steps:

- Pre-Placement*
- Solution Space Analysis*
- Constraint-Driven Floorplanning*
- Constraint-Driven Routing*
- Post-Route DRC*
- Post-Route Analysis*

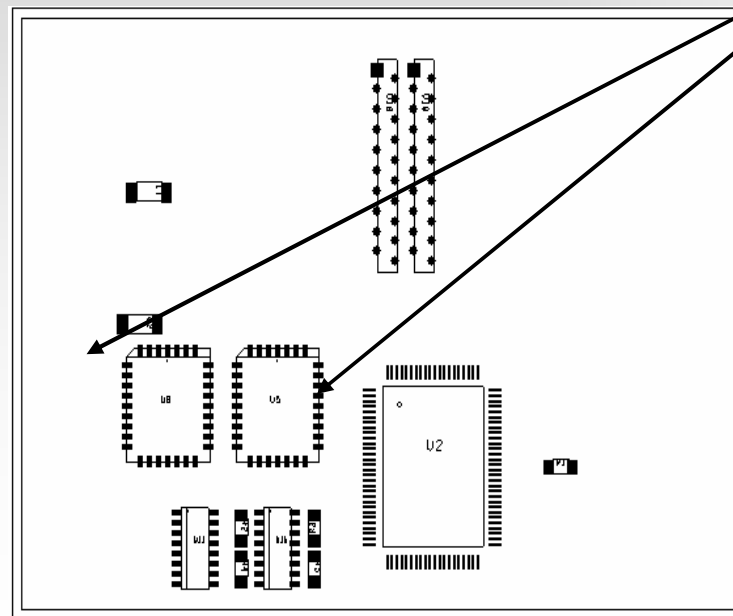


Design Flow: Pre-Placement

Standard form factors, mechanical restrictions, and standard practices often predefine locations of critical components.

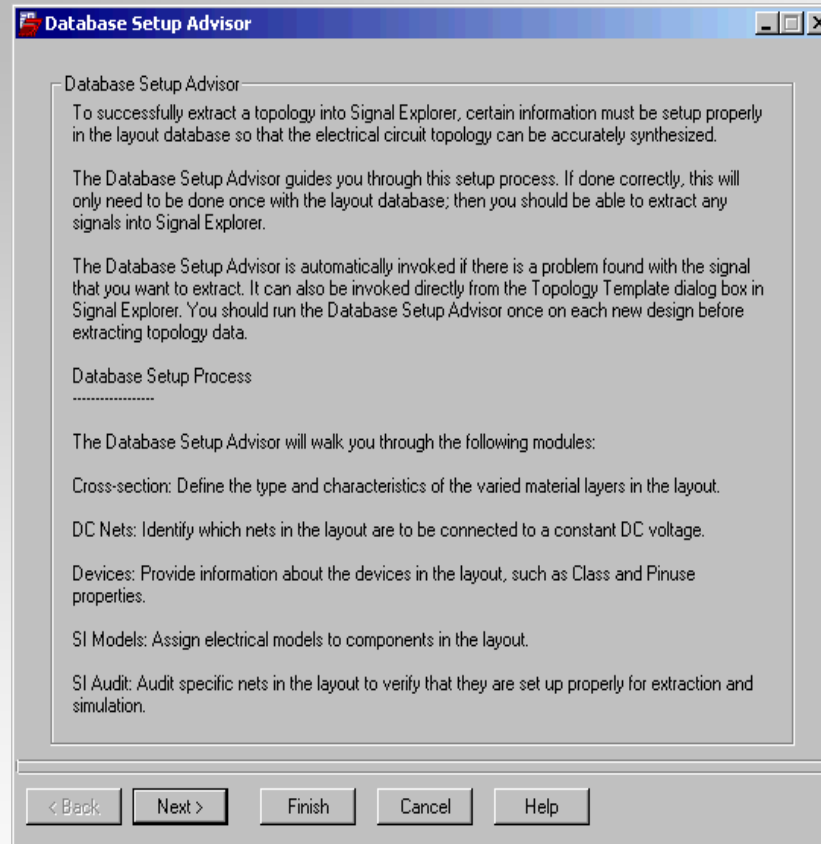
Electrical design must start with these requirements, or present a strong case why things should be changed.

Pre-placed design is usually created by the CAD group as a starting point for design.



Chip set placement
predetermined

Database Setup Advisor



Ø The first screen of the Database Setup Advisor.

Ø Explains the use of Database Setup Advisor.

Ø Describes the steps you must take to set up the database correctly.

Ø “Set up Right, Set up Once”.

Defining the Layout Cross-Section

Layout Cross Section

Cross Section

	Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)	Impedance (ohm)
1		SURFACE	AIR								
2	TOP	CONDUCTOR	COPPER	1.2	595900	1	0	<input type="checkbox"/>		5	65.777
3		DIELECTRIC	FR-4	5	0	4.500000	0				
4	INTERNAL1	PLANE	COPPER	1.2	595900			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
5		DIELECTRIC	FR-4	14	0	4.500000	0				
6	INTERNAL2	PLANE	COPPER	1.2	595900			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
7		DIELECTRIC	FR-4	5	0	4.500000	0				
8	BOTTOM	CONDUCTOR	COPPER	1.2	595900	1	0	<input type="checkbox"/>		5	65.777
9		SURFACE	AIR								

Designates the currently selected layer as a shield layer. The shield layer prevents the electrical signals from the two adjacent layers from interacting with each other.

Activate Differential Mode
Layout Cross-Section Editor

Differential Mode

Total Thickness: 28.8 MIL

Stripline Layer Dielectric: [Determined Automatically]

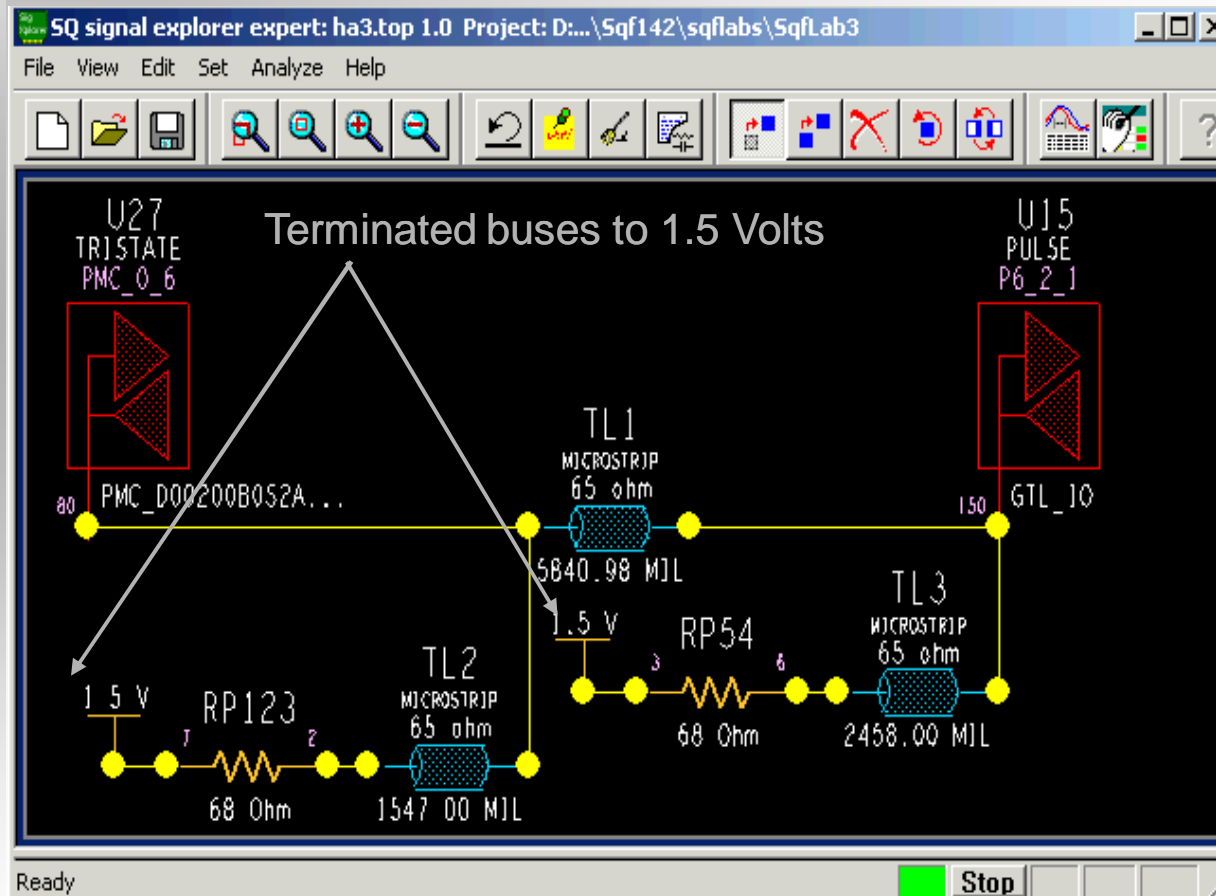
Dielectric Constant: []

Loss Tangent: []

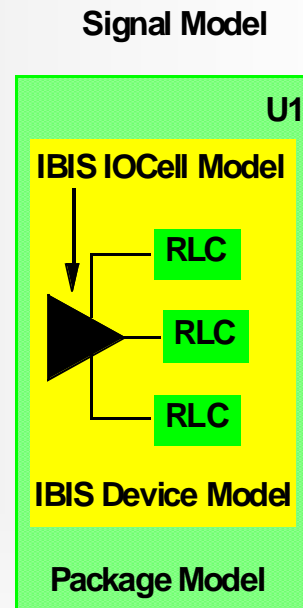
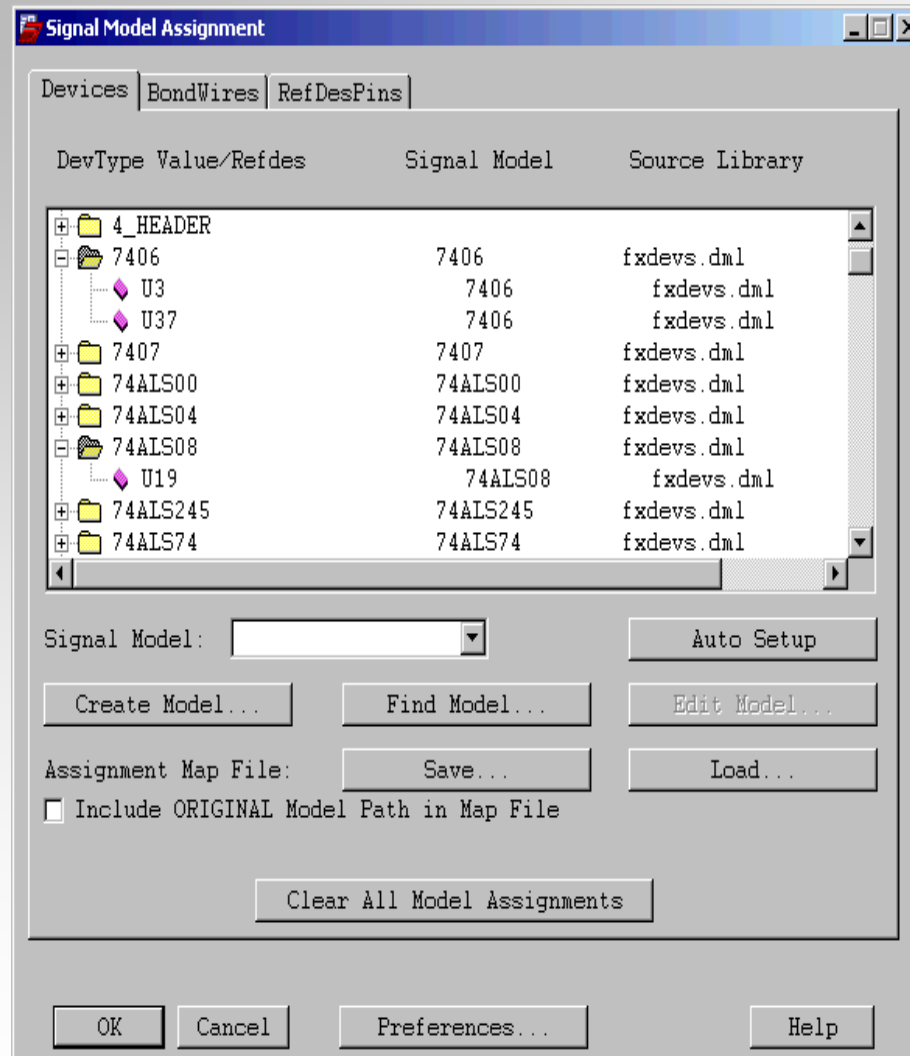
OK Apply Cancel Help

DC Voltages

SPECCTRAQuest SI Expert needs source voltages for terminators and capacitors to build an electrically correct circuit.

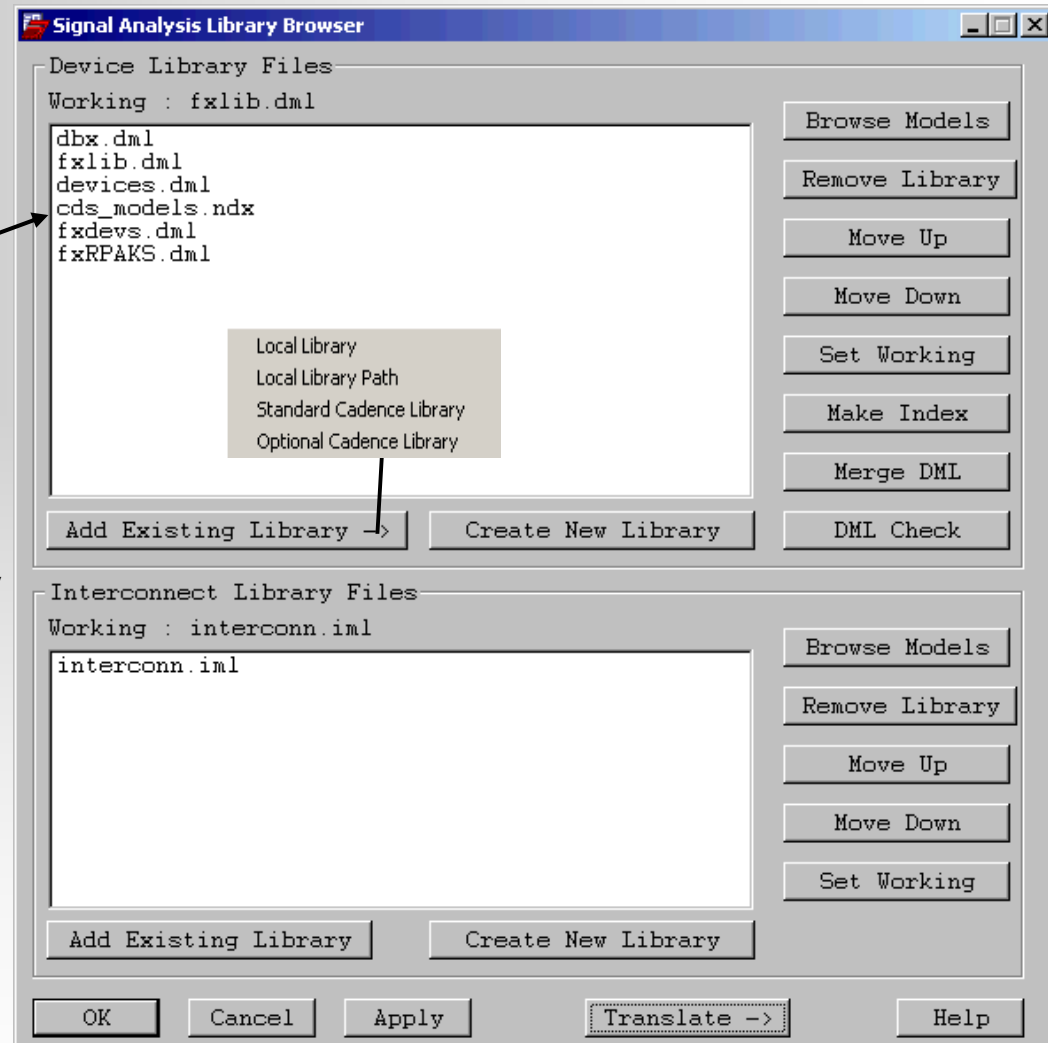


Signal Model Assignment Form



Translating and Adding Libraries

An Index file (.ndx) is a group of library files that have been merged and indexed together. You can use the models for simulation, but cannot modify the index file in any way.



You can translate these types of signal models to SPECCTRAQuest format.



Ibis2signoise
quadsignoise
FAR SIGHT

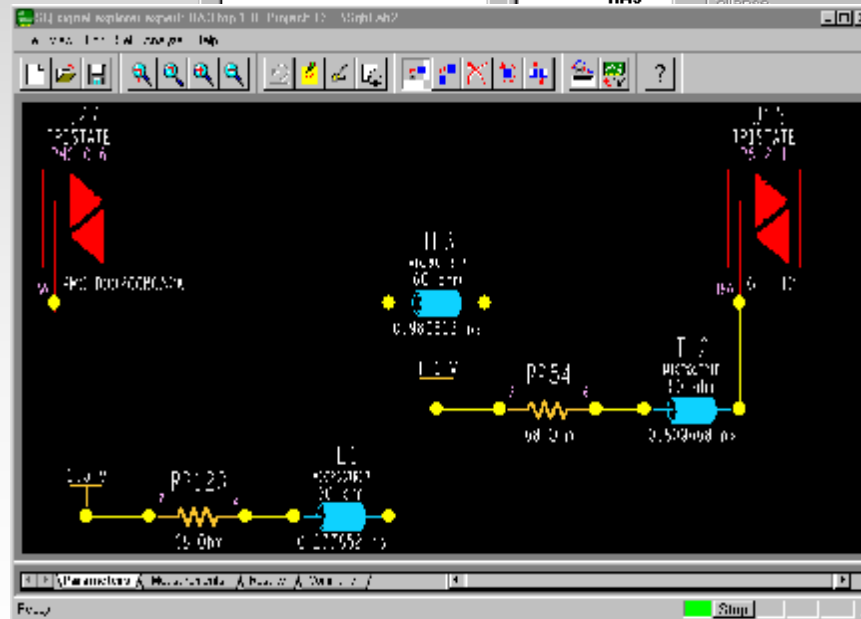
华清远见

Pre-Route Template Extraction

The Xnet includes the drivers, receivers and interconnects of an extended net.

The screenshot shows the 'Constraint Manager' window with a table of objects. A context menu is open over the 'HA3' through 'HA9' rows. The table has columns for 'Objects', 'Referenced Electrical CSet', 'Pin Pairs', and two sets of 'Prop Delay' (Min, Actual, Margin) with units in ns.

Objects	Referenced Electrical CSet	Pin Pairs	Prop Delay			Prop Delay		
			Min ns	Actual	Margin	Max ns	Actual	Margin
@FX.FX(SCH_1):GNT								
@FX.FX(SCH_1):HA								
HA3								
HA4								
HA5								
HA6								
HA7								
HA8								
HA9								



华清远见

SQ Signal Explorer Expert Parameters Tab

The screenshot displays the SQ Signal Explorer Expert Parameters Tab. The top part shows a circuit diagram with components like U27 (TRI STATE), U15 (PULSE), RP123, RP54, and transmission lines TL1, TL2, and TL3. The bottom part shows a table of parameters for the selected component (TL1).

Name	Value	Count
CIRCUIT		1
tlineDelayMode	length	
userRevision	1.0	
STARTLB2		
RP54		1
RP123		1
TL1		1
impedance	65 ohm	1
length	5840.98 MIL	1
traceGeometry	Microstrip	1
velocity	5567.72 mil/ns	1
TL2		1

Toggle to display the units on the TLine to Length or Time.

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SQ Signal Explorer Expert Results Tab

The screenshot displays the SQ Signal Explorer Expert Results Tab. The top portion shows a circuit diagram with components U27 (TRISTATE), U15 (PULSE), TL1, TL2, and TL3, along with resistors RP123 and RP54. The bottom portion is a table of results.

SimID	Driver	Receiver	Cycle	FTSMODE	TL3.length [MIL]	TL3. imp	Monotonic	Overshoot High	Overshoot Low	SwitchDelay Fall	SwitchDelay Rise
34	STARTLB2.U27.80	STARTLB2.U15.150	1	Slow	1000	60	PASS	1501.4	260.436	0.90171	1.13658
55	STARTLB2.U15.15	STARTLB2.U27.80	1	Fast	2000	60	PASS	1501.59	141.176	1.05547	1.26647
128	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	0	70	PASS	1511.49	107.319	0.76736	0.7638
63	STARTLB2.U15.15	STARTLB2.U27.80	1	Fast	0	65	PASS	1501.22	192.954	0.505873	0.6876
92	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	1000	65	PASS	1505.21	72.228	0.94586	0.94268
166	STARTLB2.U27.80	STARTLB2.U15.150	1	Slow	2000	70	PASS	1510.47	288.628	0.55381	0.75522
91	STARTLB2.U15.15	STARTLB2.U27.80	1	Fast	1000	65	PASS	1502.73	172.971	0.872073	1.05839
152	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	1000	70	PASS	1510.19	95.424	0.94406	0.95631
8	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	0	60	PASS	1501.98	72.6408	0.74836	0.7026
131	STARTLB2.U15.15	STARTLB2.U27.80	1	Fast	0	70	PASS	1505.49	192.486	0.873973	1.06702
148	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	1000	70	PASS	1511.46	109.321	0.76286	0.7557
60	STARTLB2.U27.80	STARTLB2.U15.150	1	Fast	2000	60	PASS	1499.41	27.8917	1.31226	1.35172

华清远见

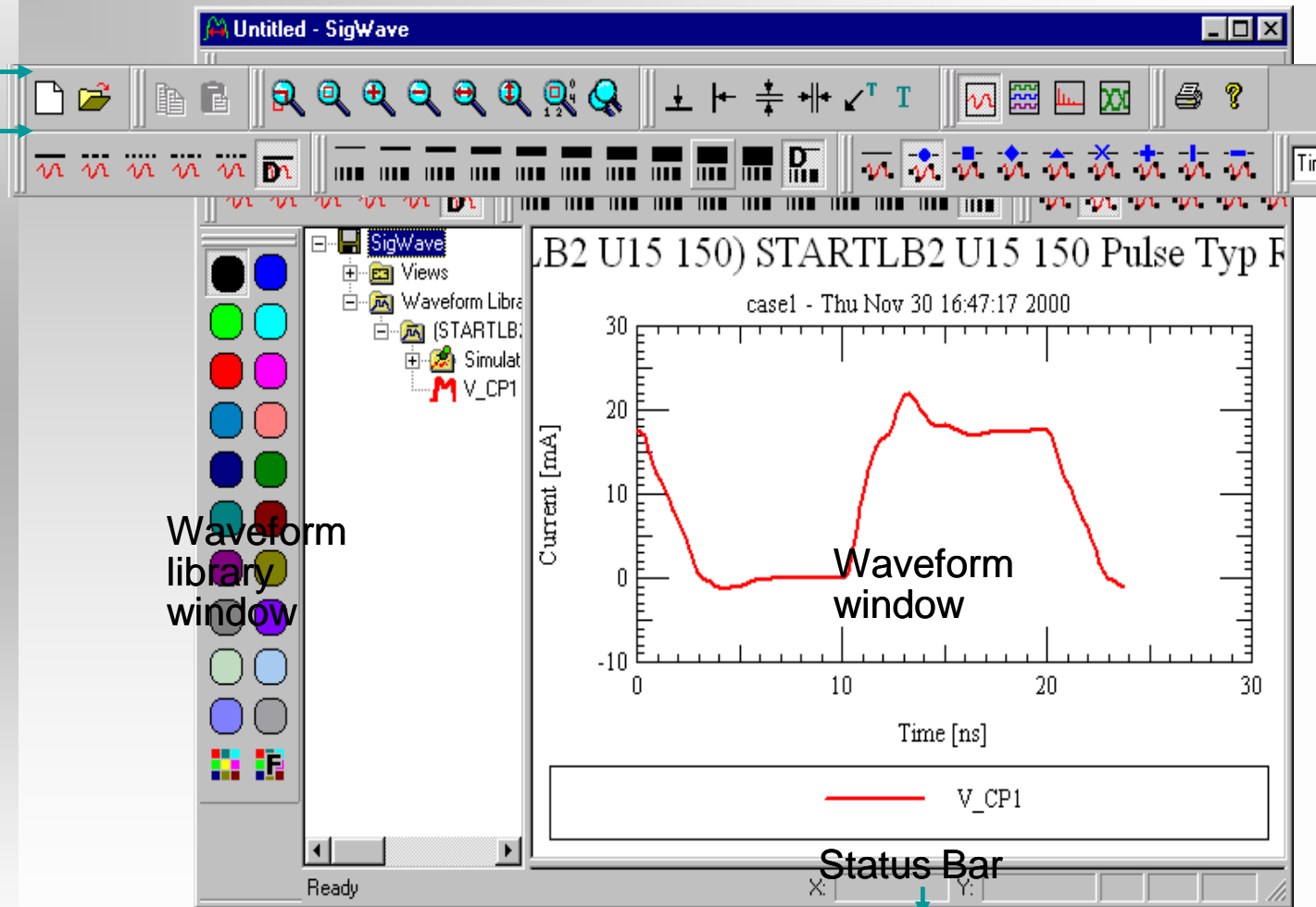
SigWave Current Waveforms

Menu Bar

Tool Bar

Waveform
library
window

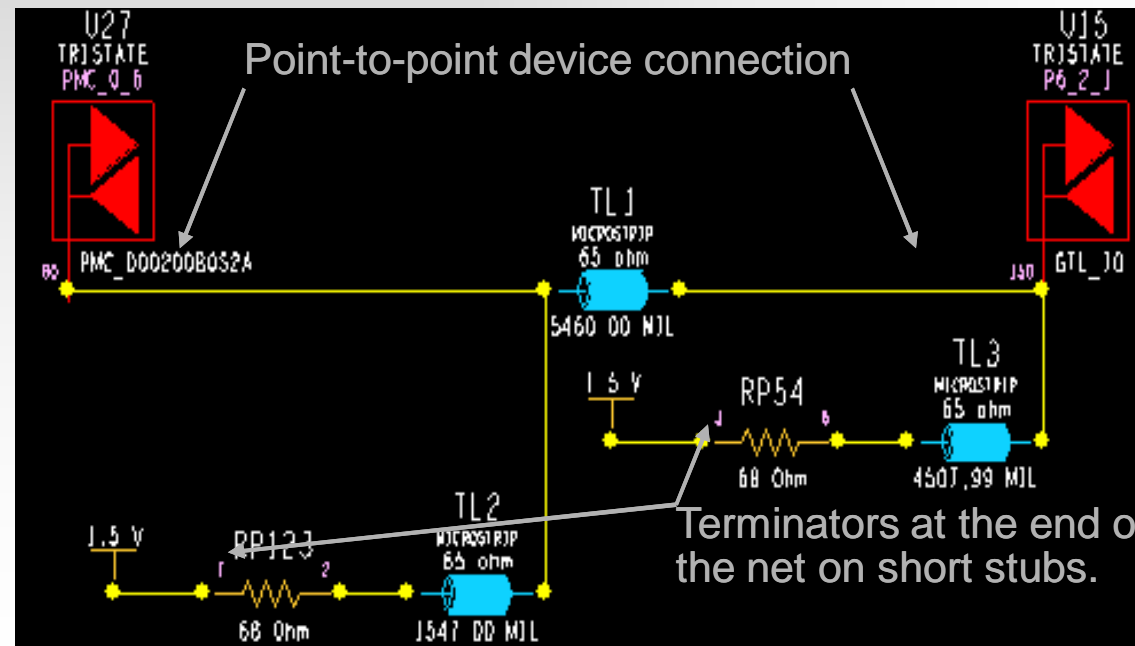
Status Bar



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Solution Space Analysis Step 1

- ∅ Extract / create topology to be analyzed.
 - ü Pin ordering
 - ü Discrete devices
 - ü Rat-T positions (if any)
- ∅ Identify / enter nominal values for all parameters.
 - ü Board impedance
 - ü Trace velocity
 - ü Terminator value
 - ü Segment lengths



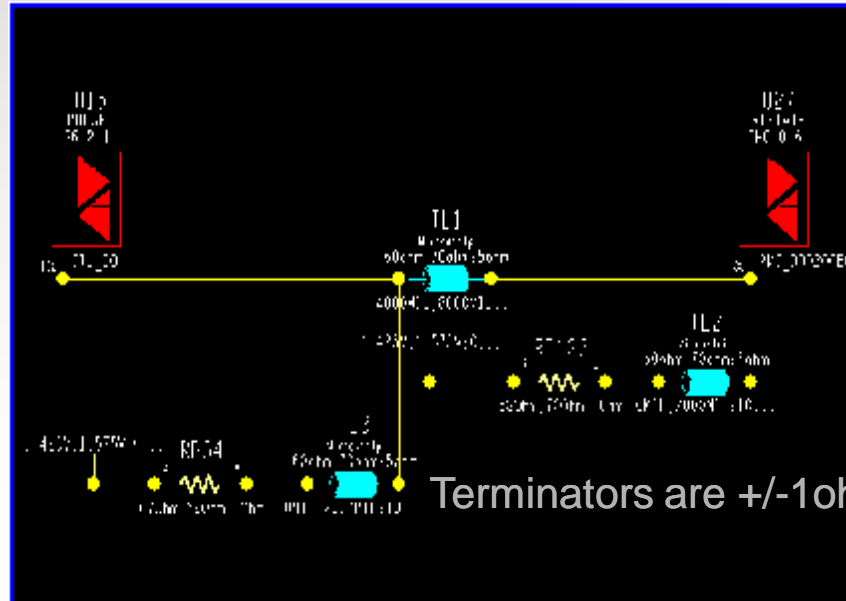
Solution Space Analysis Step 2

- ∅ Identify manufacturing variances that are to be included in the analysis.
 - ü Trace impedance (for example +/- 10%)
 - ü Trace velocity
 - ü Fast / slow components
 - ü Device values (ex. terminators)
 - ü Power supplies (if applicable)
- ∅ Identify initial ranges for “design rule” parameters.
 - ü Min / max segment lengths

1.5 volt supply is +/- 5%

Devices = Fast and Slow

Trace impedance is 65 ohms +/- 5 ohms.



Trace length varies for each TLine:
 TL1: 4000 mils to 8000 mils,
 TL2 and TL3: 0 mils to 2000 mils.

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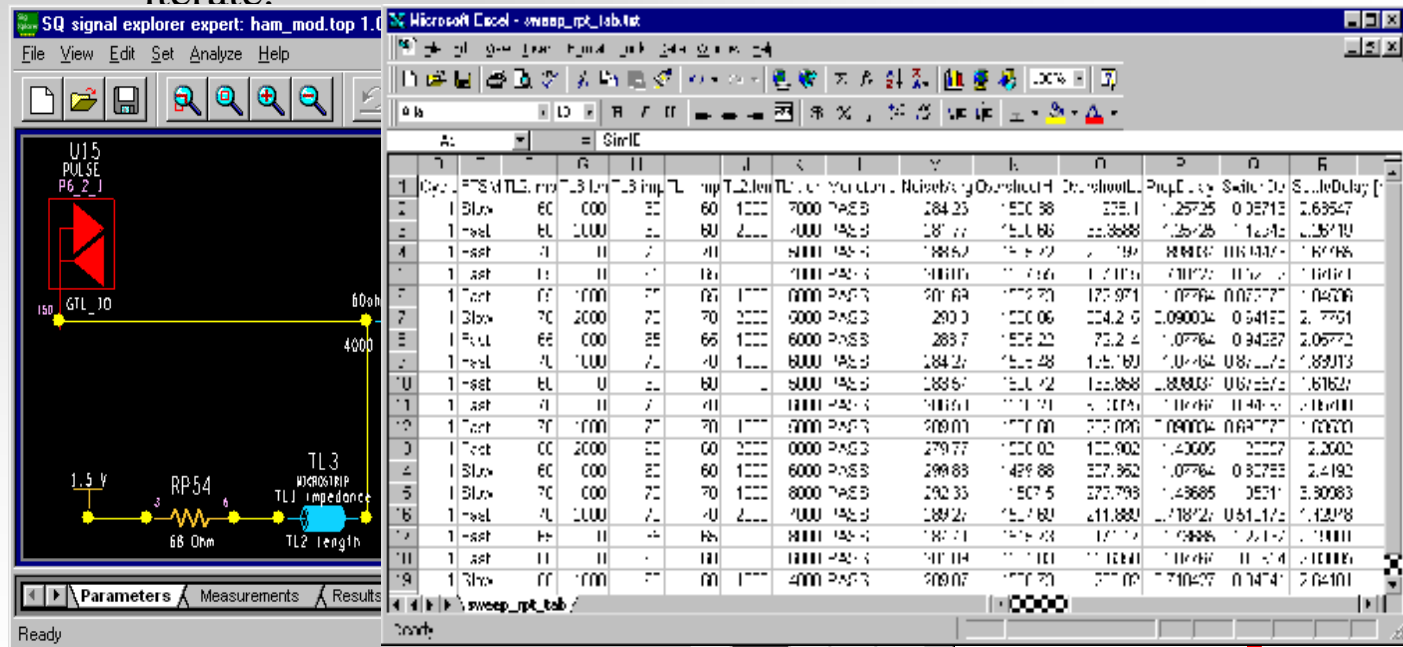
Solution Space Analysis Step 3

- ∅ Create a “master list” of all variables for analyses and their ranges.
- ∅ Identify “dependencies” between variables, based on how the design will be implemented.
 - ü Traces on the same layer have identical characteristics.
 - ü Resistors in the same RPAK match closely.
- ∅ Develop a simulation strategy based on combinations to be analyzed.

Parameter	Min	Typ	Max	# Steps
P6 Speed	Fast		Slow	2
440FX_Speed	Fast		Slow	2
TL1 Impedance	60 ohms		70 ohms	2
TL1 Velocity	5400 mils/ns		6600 mils/ns	2
TL1 Length	4000 mils		8000 mils	2
TL2 Impedance		TL1 Impedance		1
TL2 Velocity		TL1 Velocity		1
TL2 Length	0 mils		2000 mils	2
TL3 Impedance		TL1 Impedance		1
TL3 Velocity		TL1 Velocity		1
TL3 Length	0 mils		2000 mils	2
RP A Impedance	67 ohms		69 ohms	2
RP B Impedance	67 ohms		69 ohms	2
Total Combinations				512

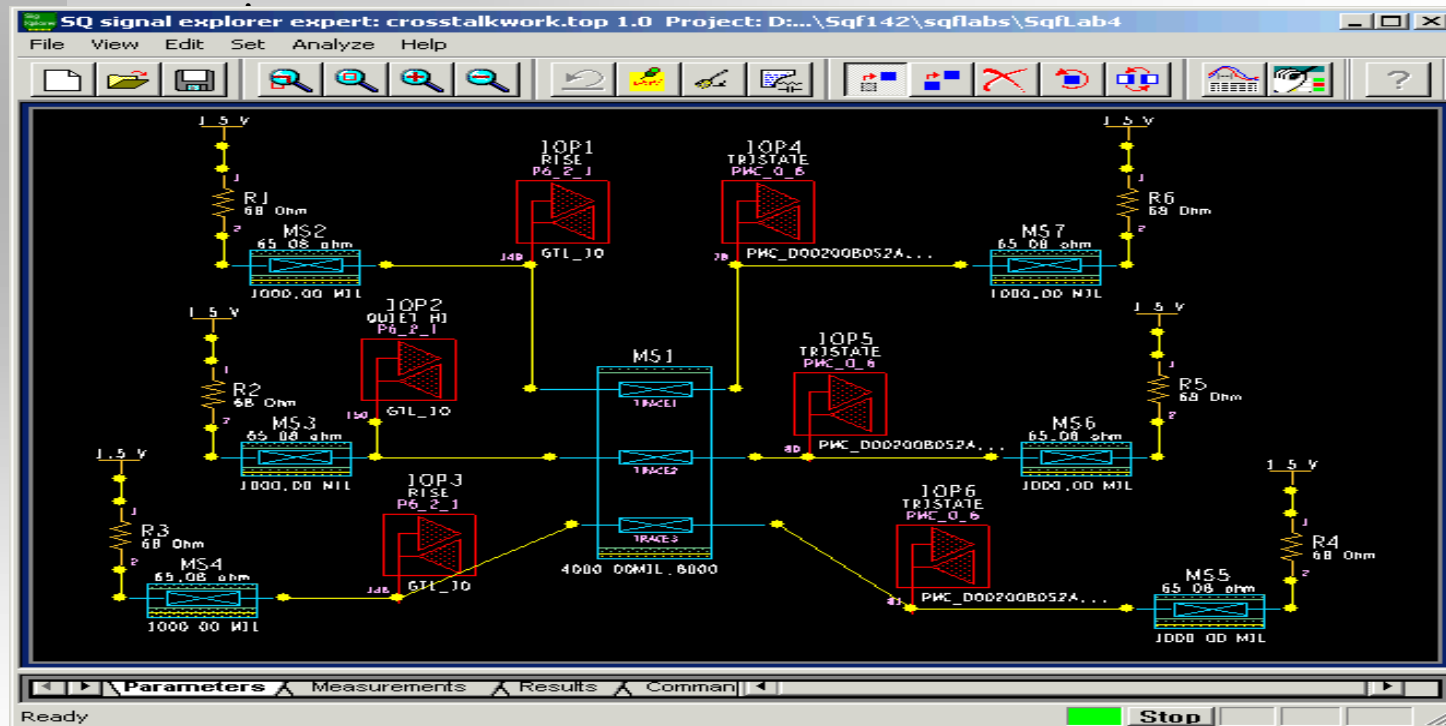
Solution Space Analysis Step 4

- Ø Run simulations and gather results.
 - ü SigXp “tabbed” report format is designed to import easily into Microsoft Excel and Access.
- Ø Evaluate results and identify “cases” (combinations of variables) that cause topology to fail (not meet design goals).
- Ø Simulate individual cases, analyze, correct design if needed, and iterate.



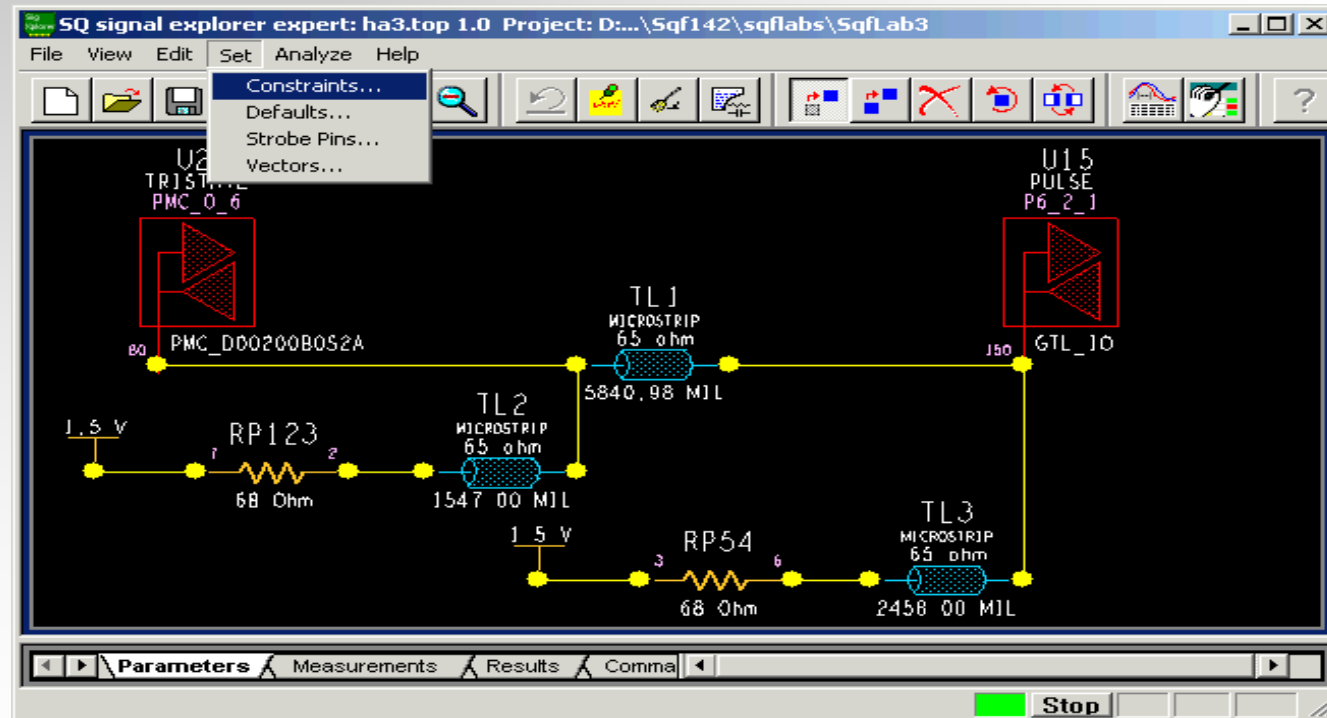
Solution Space Analysis Step 5

- ∅ The solution found thus far is a single-line solution.
- ∅ Crosstalk timing shifts must be within crosstalk budget.
- ∅ Single-line topology is modified to model coupling where appropriate.
- ∅ Different line width / spacing rules are evaluated for timing



Solution Space Analysis Step 6

- ∅ Create final topology template from analysis results:
 - ü Segment min / max lengths
 - ü Parallelism rules
- ∅ Some variances should not be included in the final topology template:



Terminators are +/-1ohm

Parametric Sweeps

The screenshot shows the SQ signal explorer expert interface. The main window displays a transmission line model (TL1) with a blue cylindrical component. Below the model is a table of parameters:

Name	Value	Count
TL1		15
impedance	60 ohm, 70 ohm: 5 ohm	3
length	4000.00 MIL, 8000.00 MIL: 1000.00 MIL	5
traceGeometry	Microstrip	1
velocity	5567.72 mil/ns	1
TL2		3

The 'Set Parameter: length' dialog box is open, showing the following settings:

- Single Value: Single Value Value:
- Linear Range: Linear Range
 - Start Value: 4000.00 MIL
 - Stop Value: 8000.00 MIL
 - Count: 5
 - Step Size: 1000.00 MIL
- Multiple Values: Multiple Values
 - Insert Value:
 - Delete Value:
 - TextEdit...:
- Expression: Expression
 - Variables: TL2.impedance, TL2.length
 - Append Var:
 - TextEdit...:

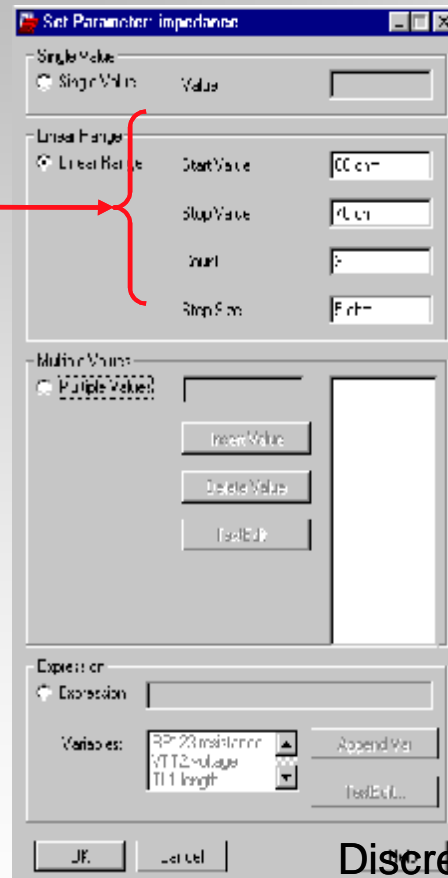
Red arrows point from the dialog box settings to the corresponding values in the software interface table and model.

Sweep parameters are chosen by setting a start and stop value. The count value determines the number of sweep count points.

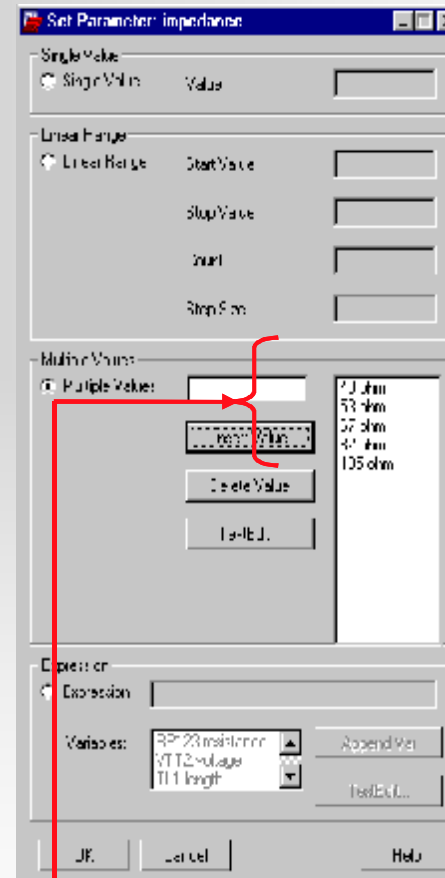
华清远见

Setting Sweep Parameters

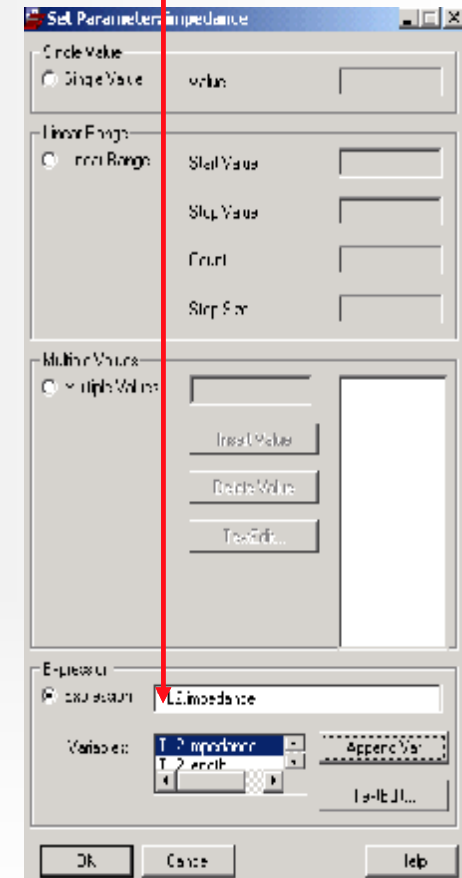
Count value determines the number of sweep count points.



Expression listed and other parameters used in the expression determine the number of sweep count points.

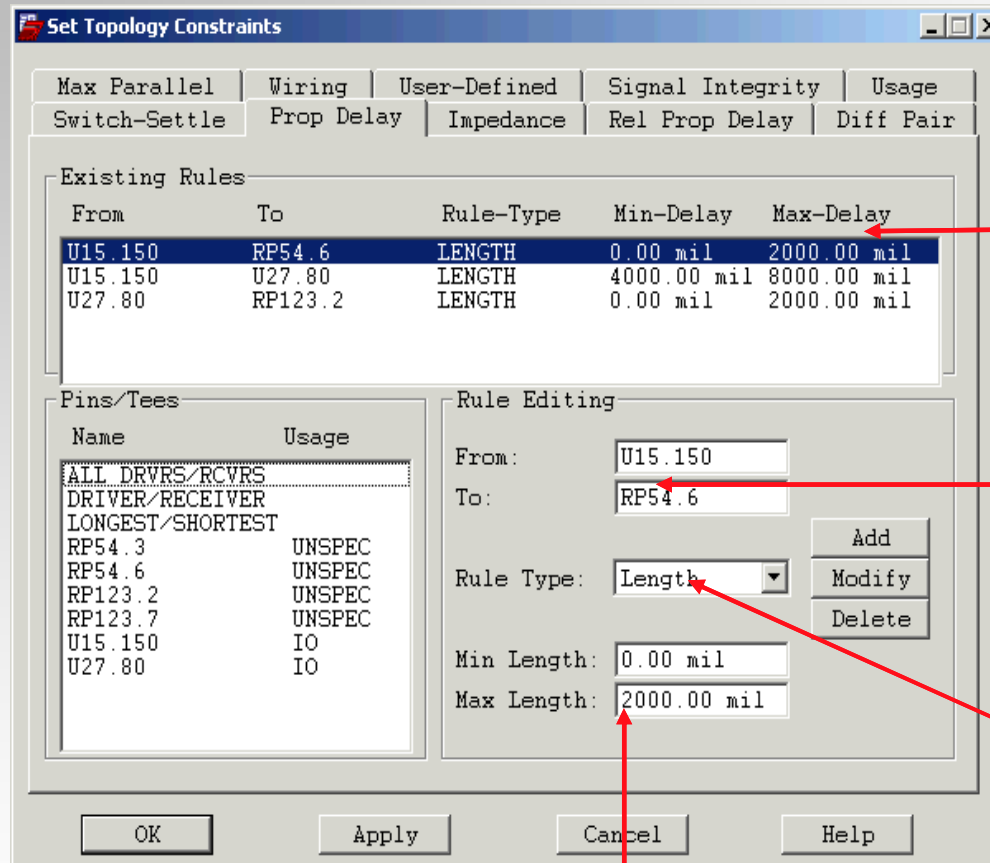


Discrete values determines the number of sweep count points.



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Assigning Prop Delay Constraints



List the Pin or Pin-Tee pairs that have delay constraints assigned in the current topology.

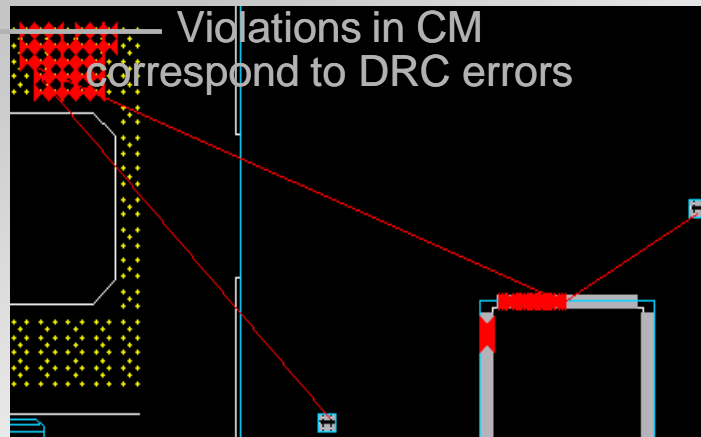
Identify the desired points between which Prop Delay constraint is to be applied.

Delay Length % Manhattan

Components are listed with their pinuse values.

Identify the desired min and max delay acceptable for this pair.

Template Applications and Constraint-Driven Placement



Constraint values

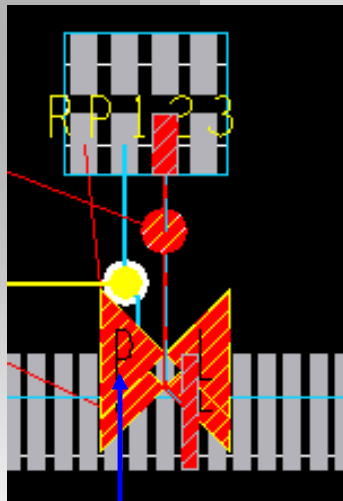
Actual manhattan routing distance

Worst case bubbles to the top

Referenced Electrical CSet	Pin Pairs	Prop Delay			Prop Delay		
		Min ns	Actual	Margin	Max ns	Actual	Margin
HA3						-17607 MIL	
HA3						-2508 MIL	
	0 MIL	4508 MIL	4508 MIL	2000 MIL	4508 MIL	-2508 MIL	
	4000 MIL			8000 MIL	5460 MIL	2540 MIL	
	0 MIL			2000 MIL	1547 MIL	453 MIL	
HA4	HA3					-17607 MIL	
U15.149:RP48.4		0 MIL	19607 MIL	19607 MIL	2000 MIL	19607 MIL	-17607 MIL
U15.149:U27.78		4000 MIL			8000 MIL	5600 MIL	2400 MIL
U27.78:RP123.3		0 MIL			2000 MIL	1538 MIL	462 MIL
HA5	HA3					-8557 MIL	
U15.140:RP124.3		0 MIL	10557 MIL	10557 MIL	2000 MIL	10557 MIL	-8557 MIL
U15.140:U27.83		4000 MIL			8000 MIL	5301 MIL	2699 MIL
U27.83:RP60.6		0 MIL	8735 MIL	8735 MIL	2000 MIL	8735 MIL	-6735 MIL
HA6	HA3					-10422 MIL	
U15.148:RP55.1		0 MIL	12422 MIL	12422 MIL	2000 MIL	12422 MIL	-10422 MIL
U15.148:U27.77		4000 MIL			8000 MIL	5720 MIL	2280 MIL
U27.77:RP123.4		0 MIL			2000 MIL	1549 MIL	451 MIL

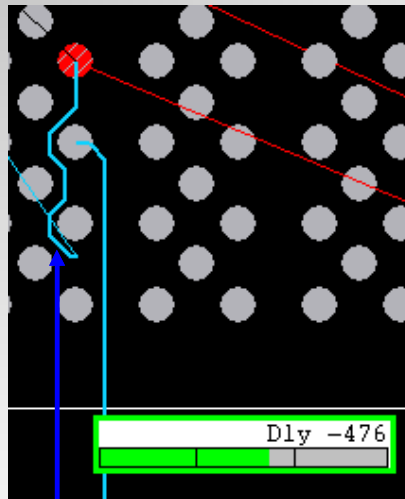
Constraint-Driven Routing

Bubble: Off



The spacing rule violation flagged off by DRC markers

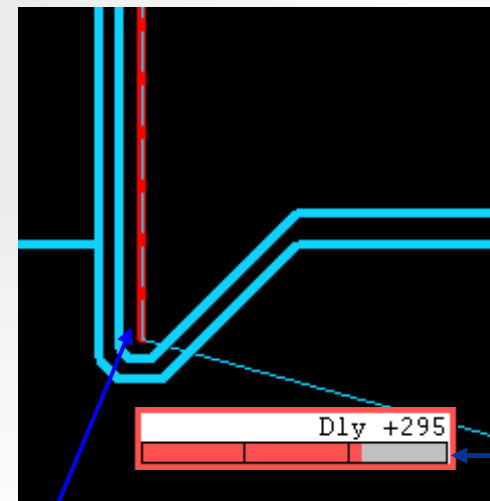
Bubble: Hug Preferred



The etch that is routed hugs the object to avoid DRC violation.

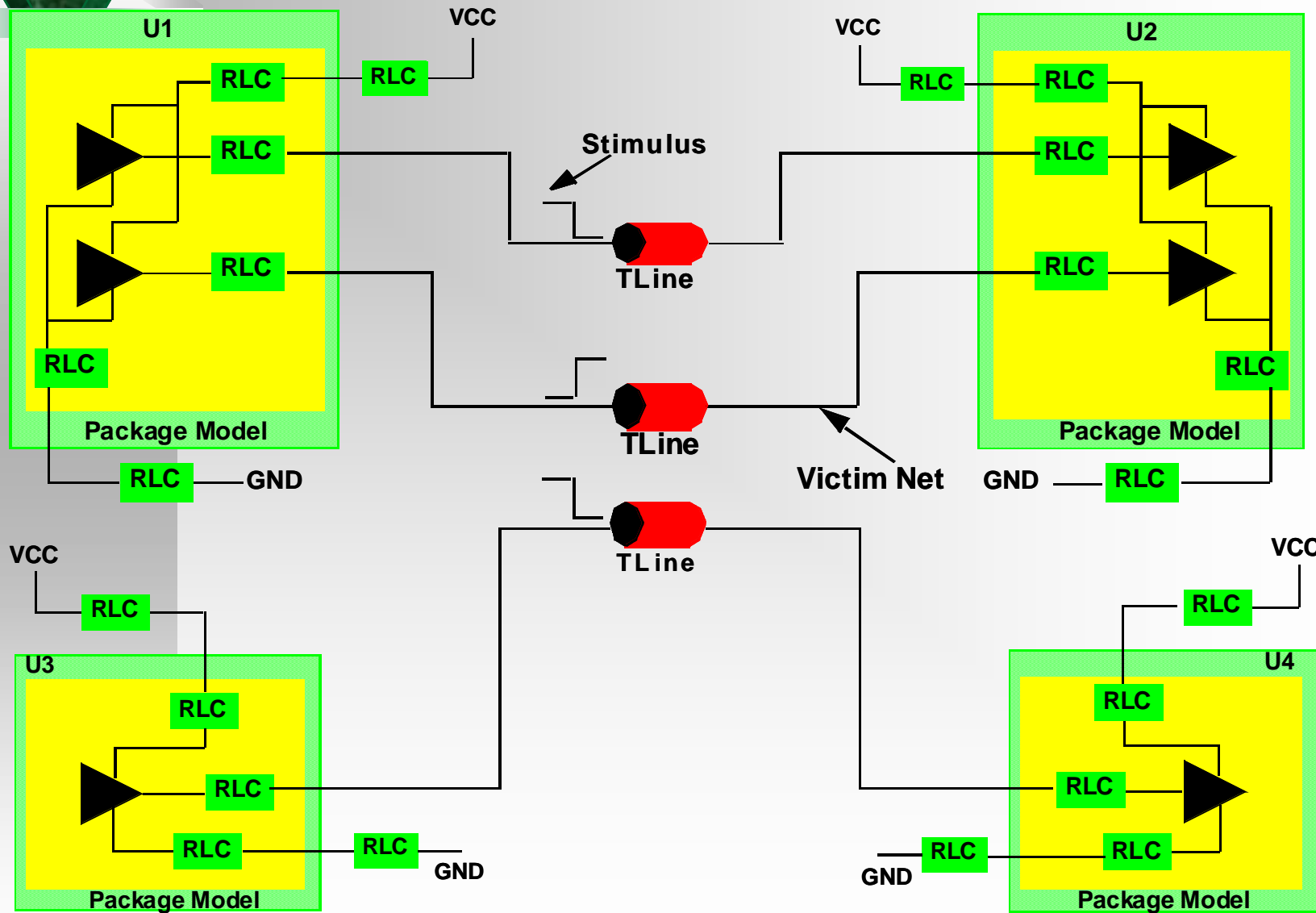
Dynamic timing meter highlights high-speed timing constraint violation.

Bubble: Shove Preferred

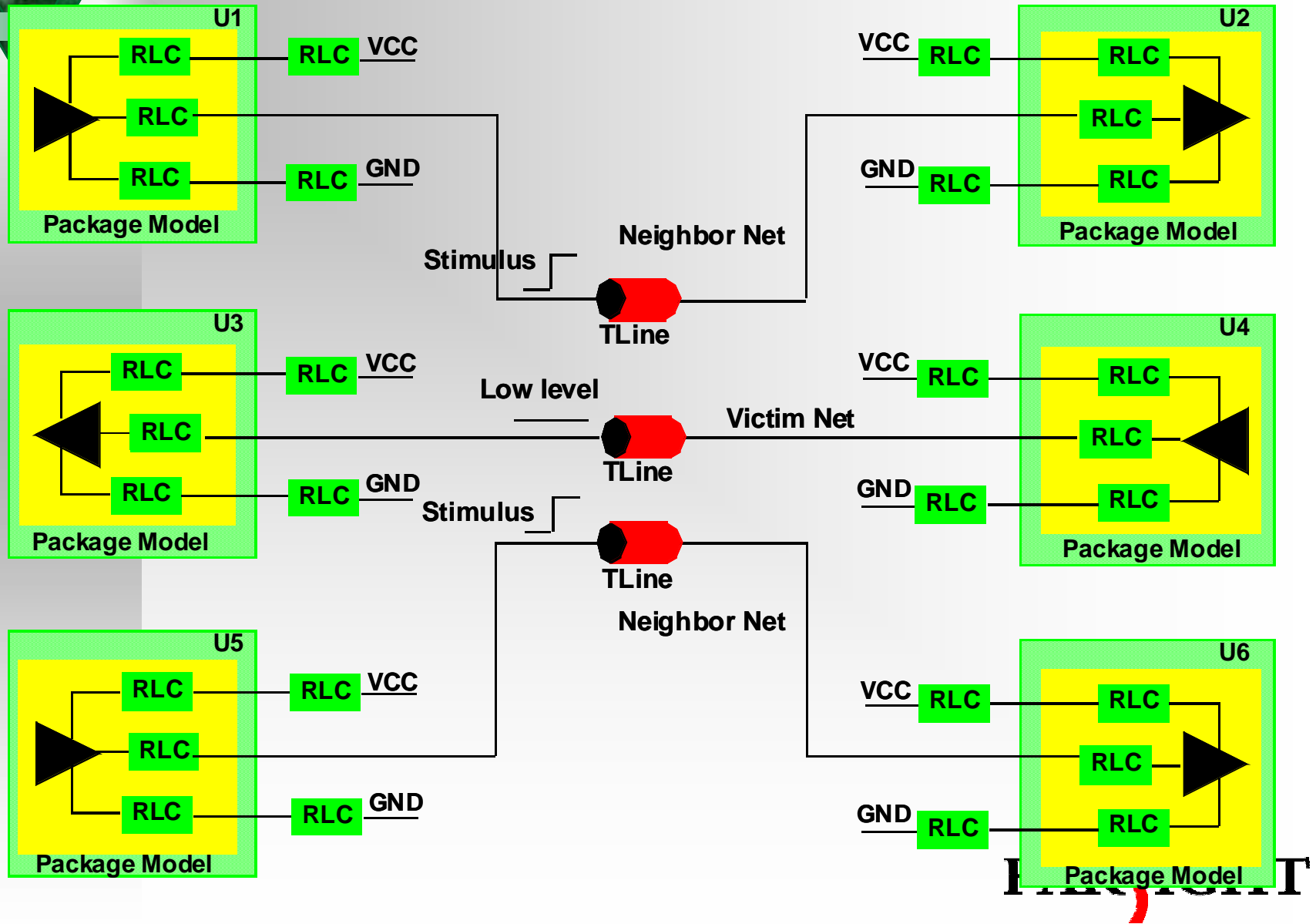


The etch that is routed pushes the existing etch to resolve DRC violation.

Post-Route DRC and Analysis



Crosstalk Simulation



华清远见

Simultaneous Switching Noise Report

Results from a SSN simulation:

```
*****
Simultaneous Switching Noise (mV) for XNet `2 COMPLETE HA4` (Typ FTSMODE)
*****
DrvR          Net          PowerBus  SSNRise  GroundBus  SSNFall
-----
COMPLETE U15 149  COMPLETE HA4  pwrctl   0          gndbus    51.54
-----

*****
Driver I/O Characteristics (Typ FTSMODE) RiseSlew/FallSlew in (mV/ns)
*****
DrvR          IOModel  Volmax  Vohmin  RiseSlew  FallSlew
-----
COMPLETE U15 149  GTL_IO  400 mV  3000 mV  271       284
-----

*****
Load I/O Characteristics
*****
Rcvr          IOModel          Vilmax  Vihmin
-----
COMPLETE U27 78  PMC_D00200B0S2AZZGHE  800 mV  1200 mV
-----

*****
Pulse Data Per Xnet
*****
XNet          PulseFreq  PulseDutyCycle  PulseCycleCount
-----
2 COMPLETE HA4  66MHz      0.5              1
-----

*****
```

System-Level Analysis

The screenshot shows the 'System Configuration Editor' window. It is divided into several sections:

- Drawings:** Contains buttons for 'Add File', 'Add BoardModel', 'Remove', 'Set Design Name', and 'Set Drawing Path'. Below these is a list of drawings: 'A complete.brd' and 'B daughter.brd'. A red oval annotation points to this list with the text 'Two layouts identified for this DesignLink'.
- Connections:** Contains buttons for 'Add', 'Remove', 'Copy', 'Set Length', and 'Set Cable Model'. Below these is a list of connections: 'DIAPINS' and 'OMETER'. A red oval annotation points to this list with the text 'Connection, length and RLGC cable model identified'.
- System Xnets Names From Design:** A dropdown menu currently set to 'A'.
- Connection PinMap:** Contains buttons for 'Add Wires', 'Remove Wires', 'Connect by Component', and 'TextEdit PinMap'. Below these are 'Set From Pin(s)' and 'Set To Pin(s)' buttons.
- Wire(s) Table:** A table with three columns: 'Wire(s)', 'Set From Pin(s)', and 'Set To Pin(s)'.

Wire(s)	Set From Pin(s)	Set To Pin(s)
1 - 49	A J12 A1 - A J12 A49	B J1 A01 - B J1 A49
50 - 60	A J12 A52 - A J12 A62	B J1 A52 - B J1 A62
61 - 109	A J12 B1 - A J12 B49	B J1 B01 - B J1 B49
110 - 120	A J12 B52 - A J12 B62	B J1 B52 - B J1 B62

 - A yellow box highlights the 'Wire(s)' column, with a red oval annotation 'Number of wires in this connection'.
 - A cyan box highlights the 'Set From Pin(s)' column, with a red oval annotation 'Connections on the first board'.
 - A magenta box highlights the 'Set To Pin(s)' column, with a red oval annotation 'Connections on the second board'.
- Buttons:** 'OK', 'Cancel', and 'Help' are located at the bottom of the window.

Differential Pair Design Exploration

Constraint Manager (connected to SPECTRAQuest SI Expert 15.0) - [Nets: Routing]

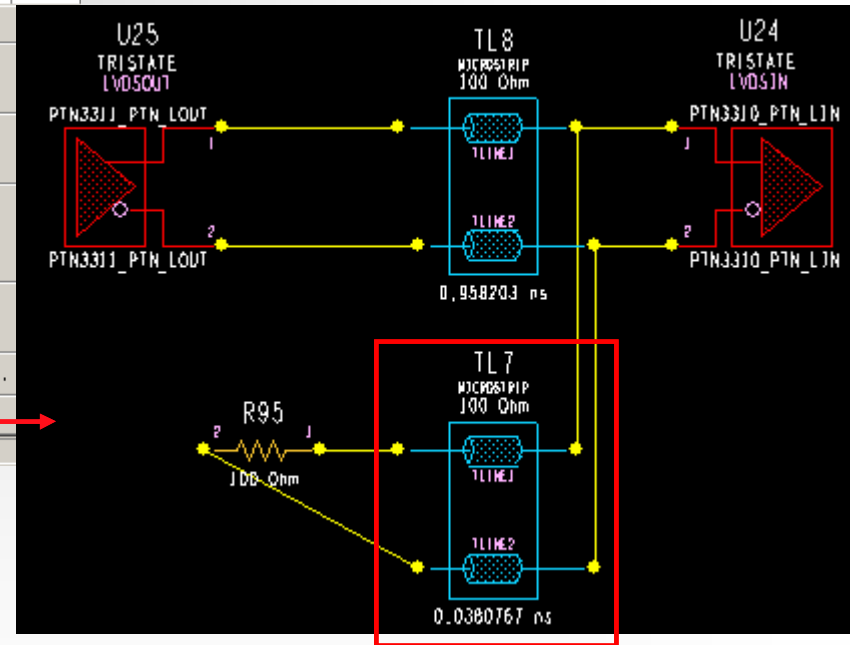
File Edit Objects Column View Analyze Audit Tools Window Help

Electrical Constraint Set

- Signal Integrity
- Timing
- Routing
- All Constraints
- Net
 - Signal Integrity
 - Timing
 - Routing
 - Wiring
 - Impedance
 - Min/Max Propagation Delay
 - Total Etch Length
 - Differential Pair
 - Relative Propagation Delay
 - Custom Measurement

Objects	Referenced Electrical CSet	Gather Contro
XD5		
XD6		
XD7		
@FX.FX(SCH_1):XTAL		
PWRGD		
DIFFNET1		
NET1_N		
NET1_P		
DIFFNET2		
NET2_N		
NET2_P		
DIFFNET3		
NET3_N		
NET3_P		
A20M		
ACK		
AEN		
AENR		
AERR		
AFD		
AFDR		
Total Etch Length		

Diff Pair: DIFFNET1



Extracted Ideal TlineCoupled model

华清远见

Custom Stimulus to Analyze Differential Pair Topology

IO Cell (U25) Stimulus Edit

Stimulus State

- Pulse
- Quiet Hi
- Rise
- Quiet Lo
- Fall
- Tristate
- Custom

Terminal Info

Terminal Name: DATA

Stimulus Type: SYNC

Stimulus Name: NONE

Measurement Info

Cycle(s): 1

Terminal Offset: 0 ns

Stimulus Editing

Frequency	Init	Switch At	Pattern	Tr(0-100%)	Tf(0-100%)
400 MHz	0	BOTH	1001 0011 1100 1010	0.583 ns	0.55 ns

CLOCKI

DATA

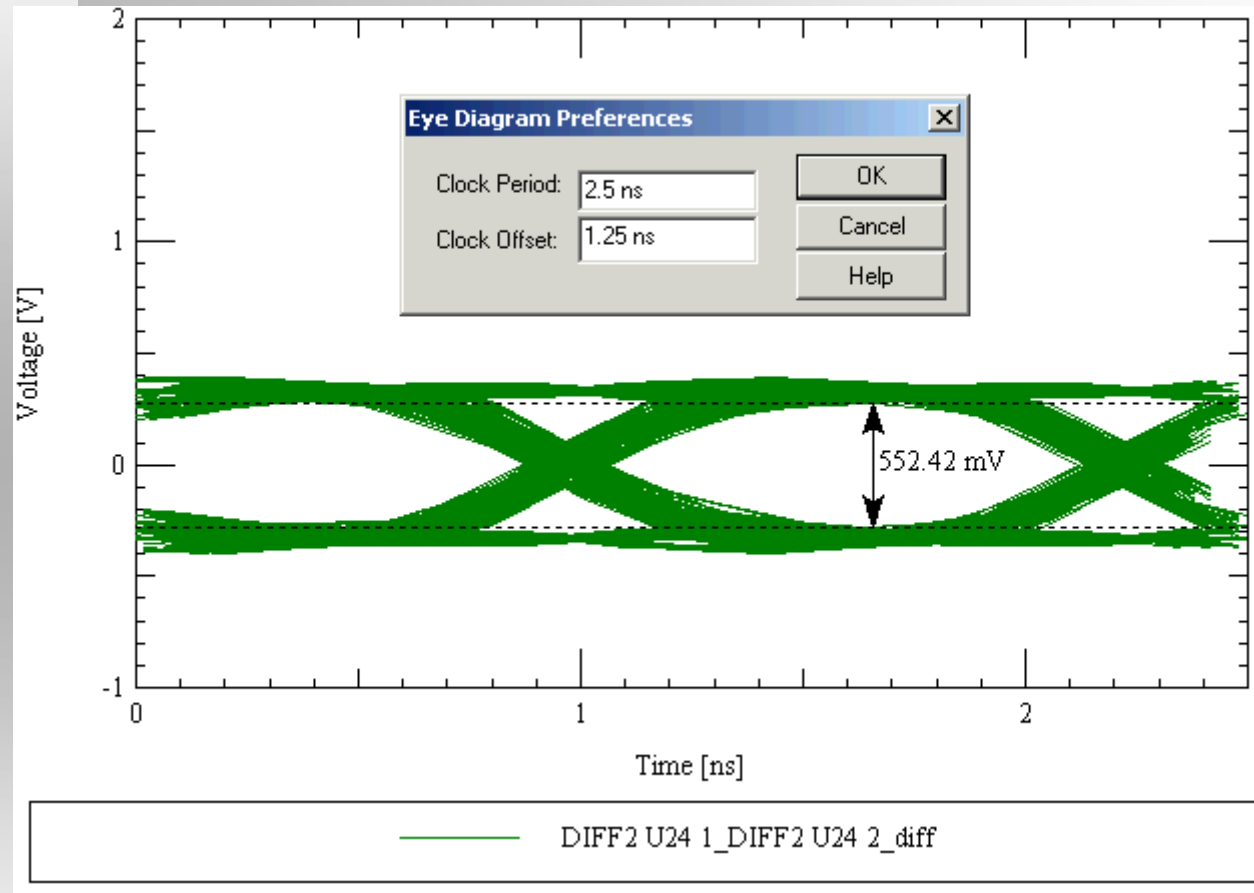
DATA_

0 ns 40 80 120 160 200

OK Apply Cancel Help

Maximum of 1024 bits

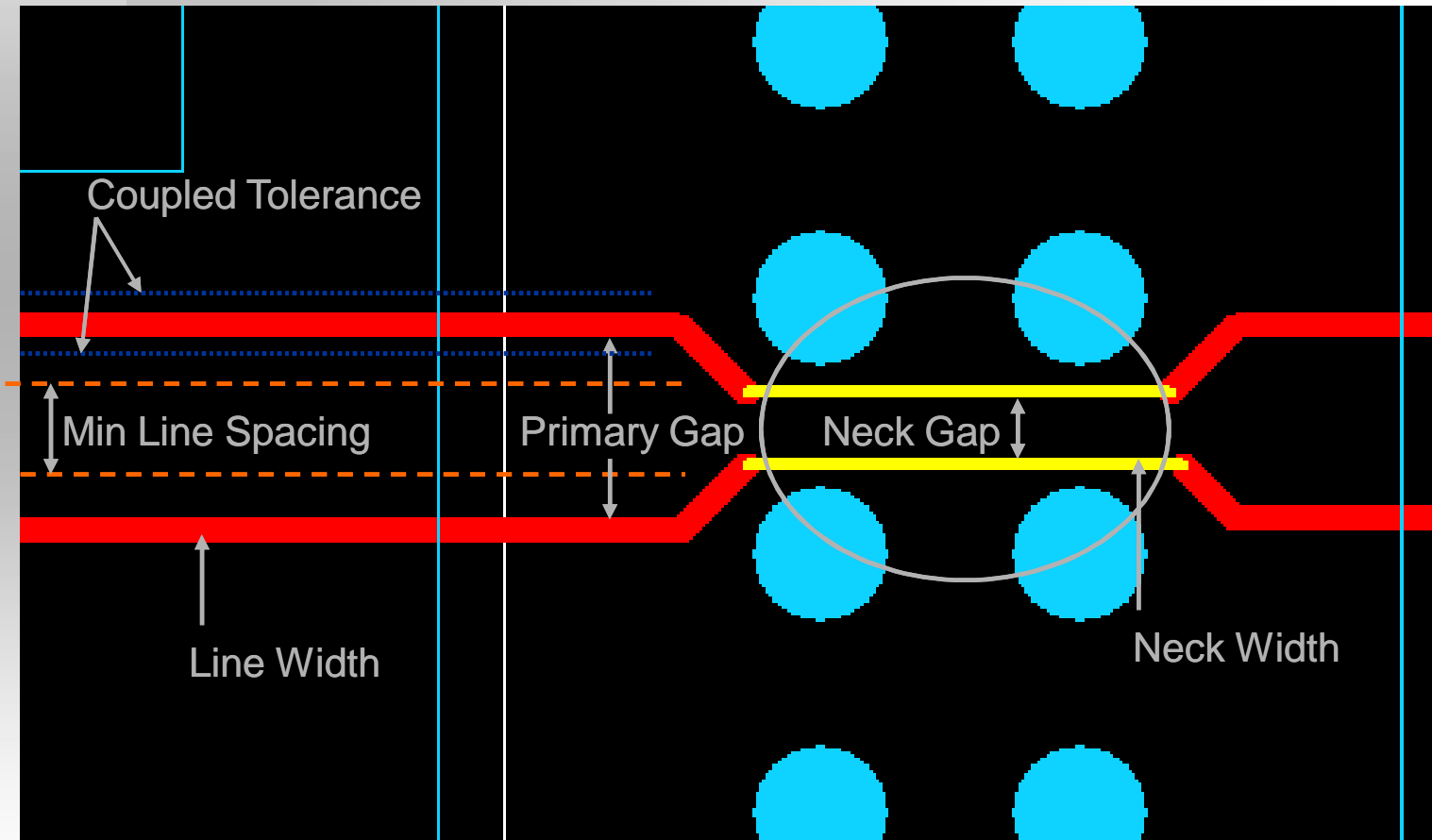
Differential Pair Topology Analysis



华清远见

Gap and Line Width

From the SPECCTRAQuest SI Expert menu, select **Route—Connect** command.



华清远见CADENCE相关课程

√ 初级班(三天)

- √ 1. Concept HDL 原理图设计
- √ 2. Allegro PCB设计
- √ 3. Librarian Expert 库管理

√ 高级班(三天)

- √ Day 1: Basic theories in high-speed PCB design
- √ Pre-Placement
- √ Extracting and Simulating Topologies
- √ Day 2: Determining and Adding Constraints
- √ Template Applications and Constraint-Driven Placement
- √ Day 3: Constraint-Driven Routing
- √ Post-Route DRC and Analysis
- √ Differential Pair Design Exploration

华清远见

让我们一起讨论！



FAR  SIGHT

The logo features the word "FARSIGHT" in white, bold, serif capital letters. A red, stylized vertical line separates the "FAR" and "SIGHT" parts. The text is centered within a dark green, textured, downward-pointing triangle that has a 3D effect with a lighter green top edge.

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谢谢！